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MS-7851

Intel -SharkBay plamform Z87

MIN ITX

Ver: 1.0(17x17)

CPU:

System Chipset:

Haswell LGA1150

Lynx Point Z87

Onboard Chip:

HD Audio Codec:ALC892

LAN-RTL8111G

SIO:Nuvoton 6779D

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) * 2 (Dual Channel)

ACPI:

PWM:

UPI

UP1649 4 Phase

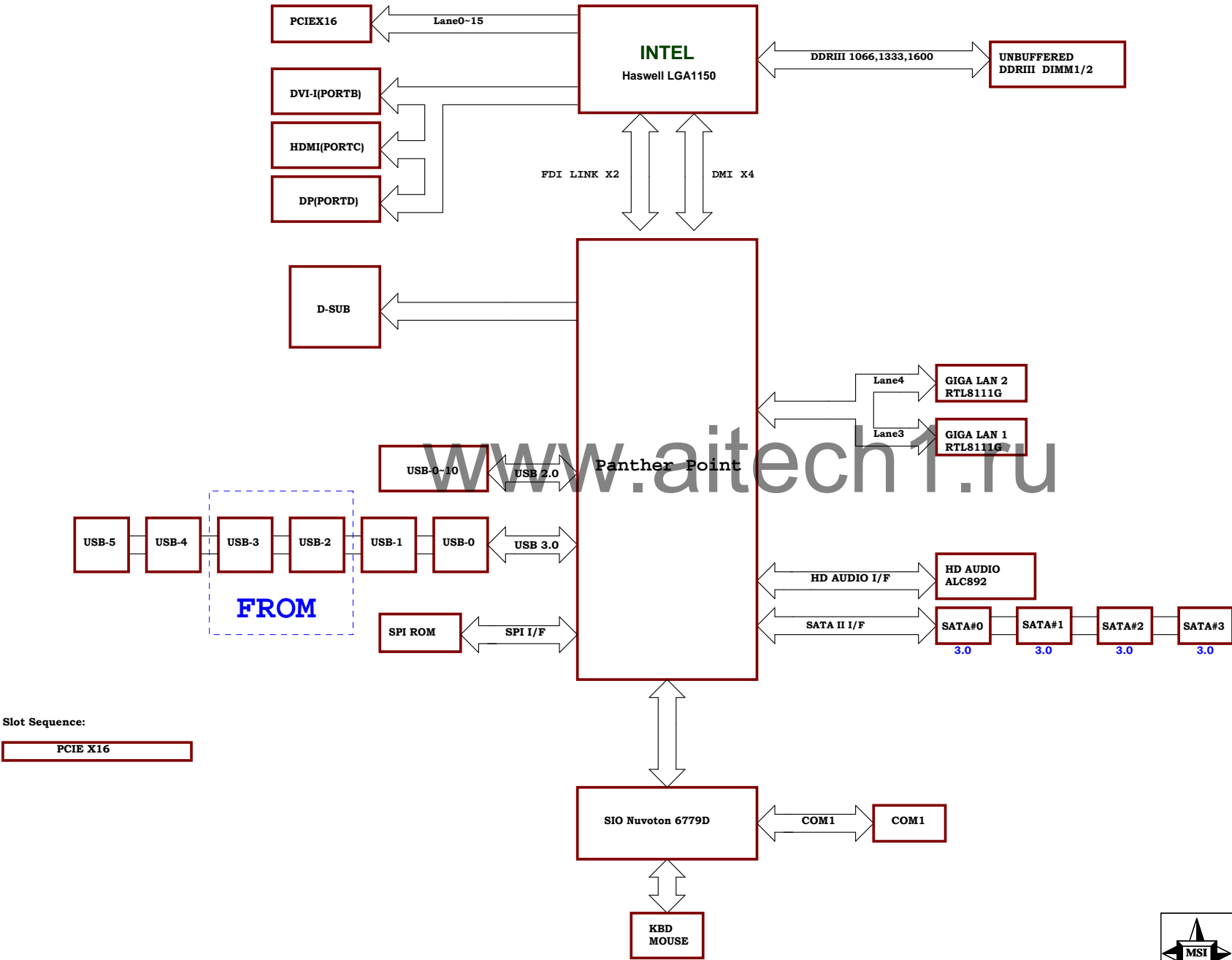
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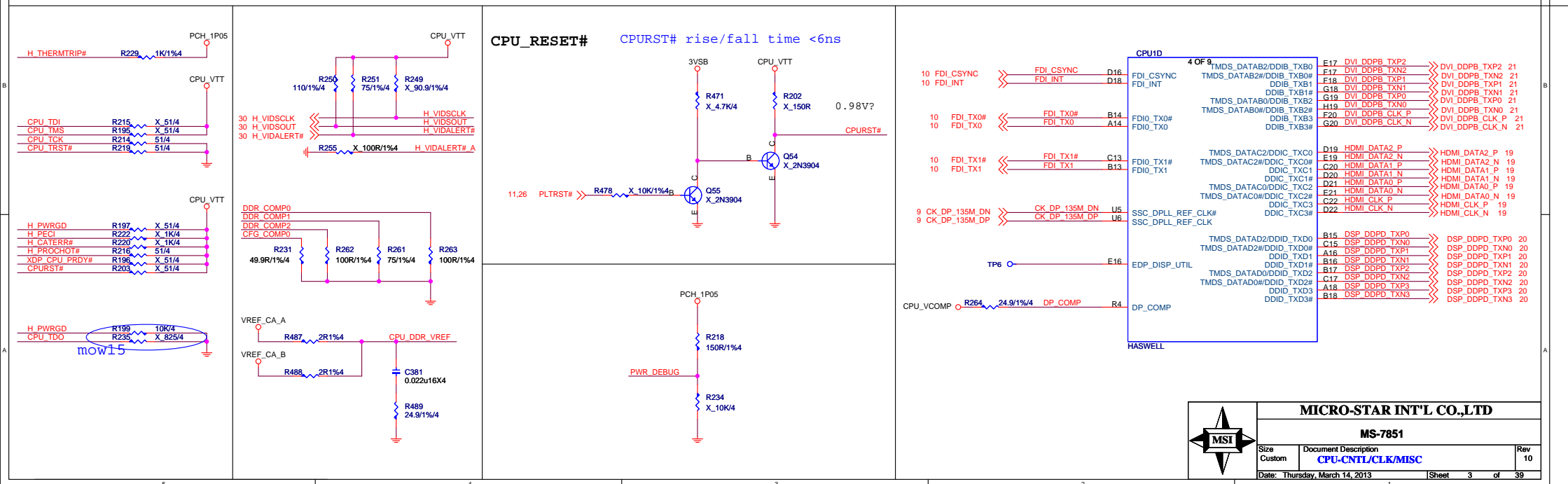
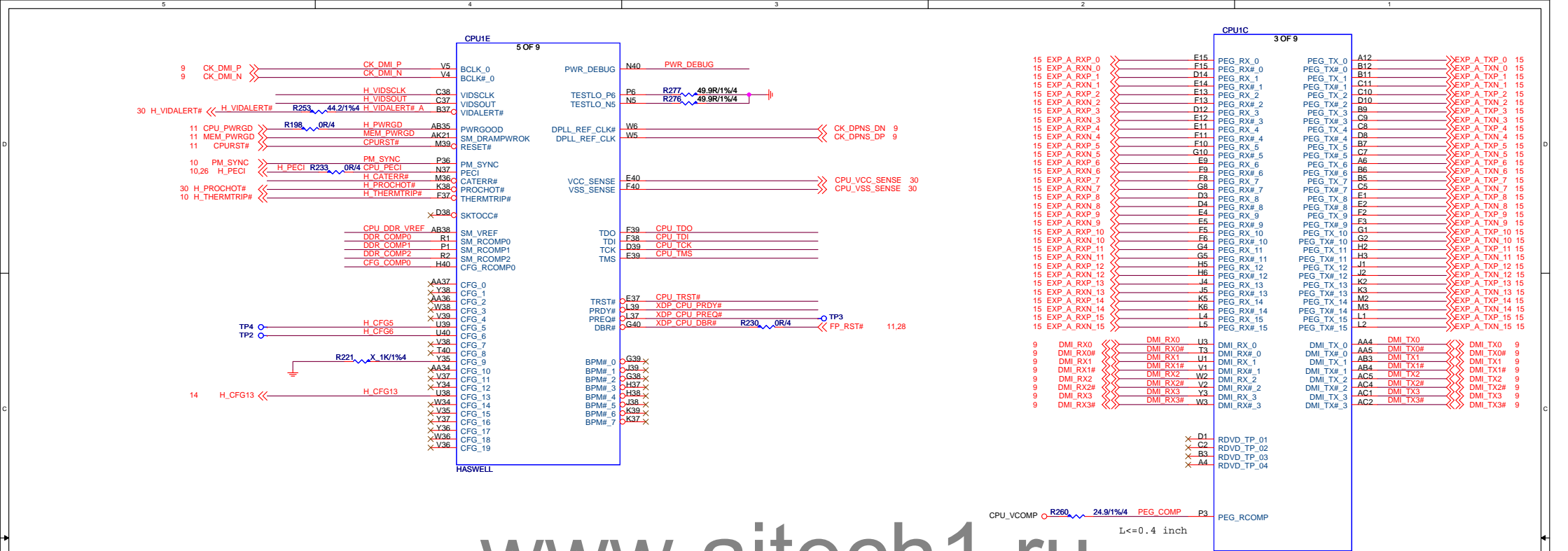
Other:

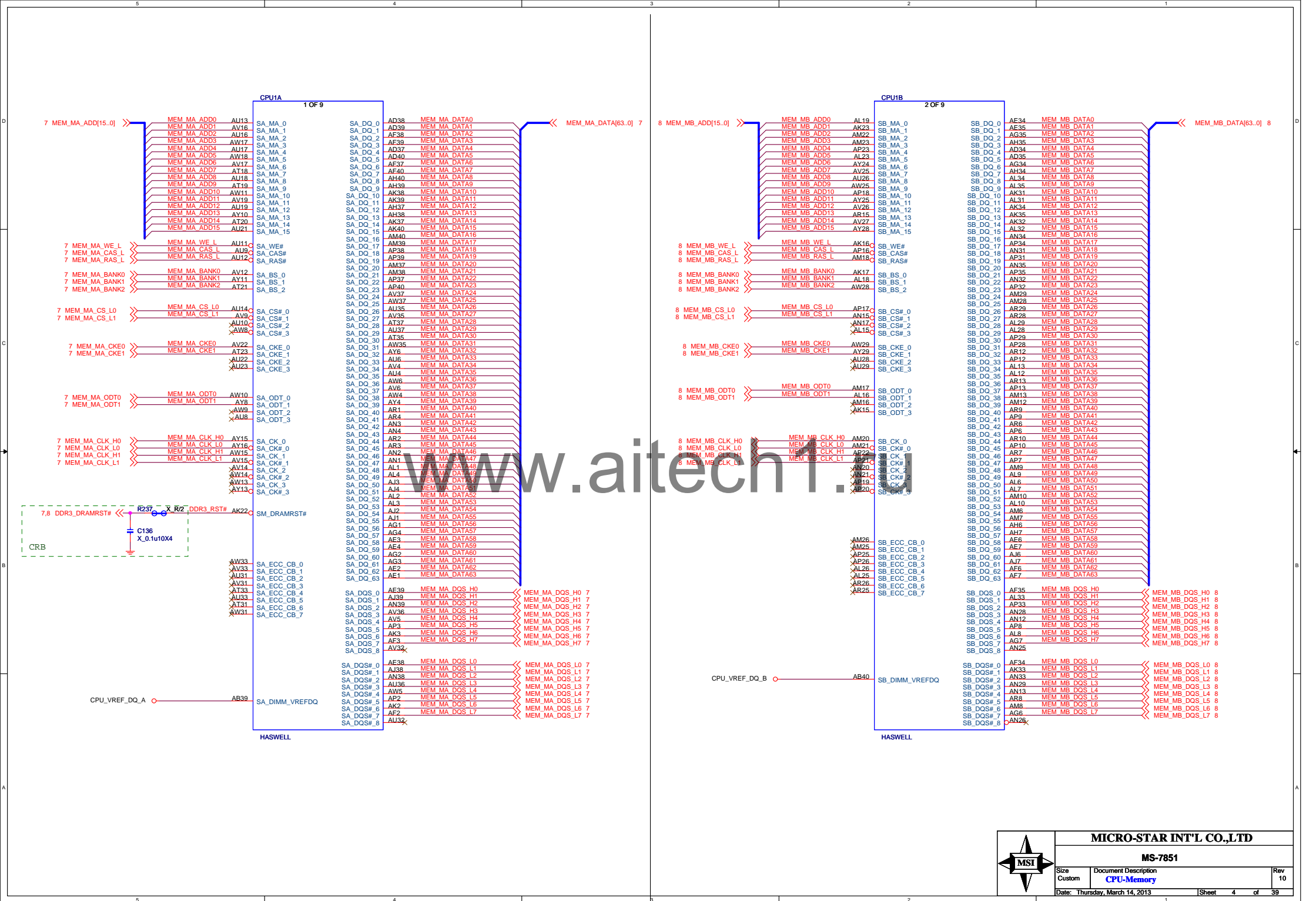
PCI Express (X16) Slot * 1

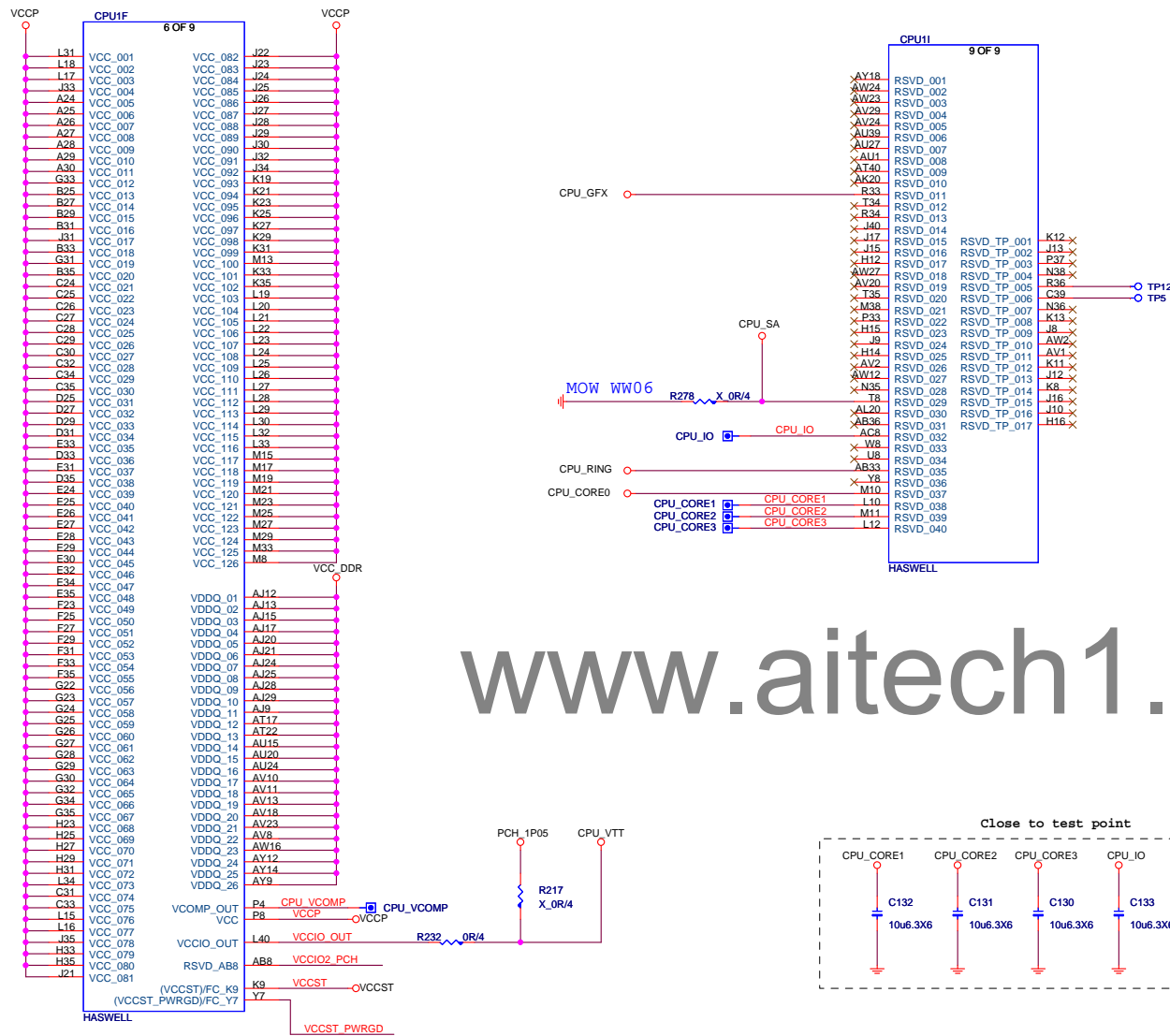
SATA3.0 x4(PCH)
REAL USB2.0 *2
FRONT USB2.0 *2
REAL USB3.0 *4
FRONT USB3.0 *2

MS-7851 Block Diagram

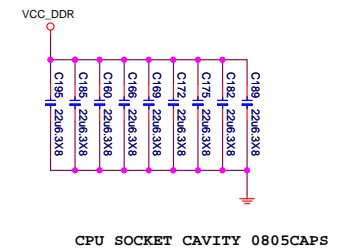




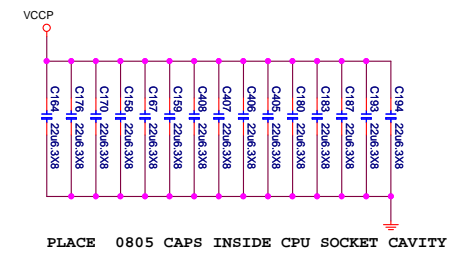




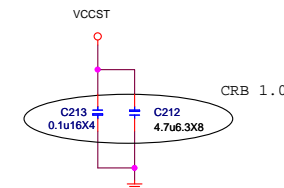
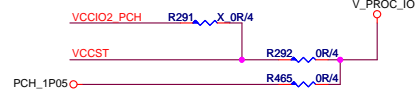
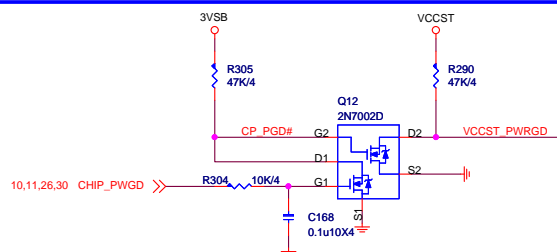
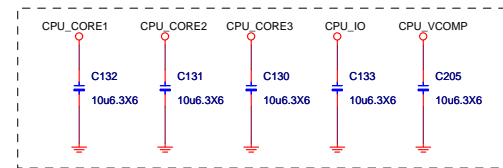
+1.5V_DDR3-Decoupling



+CPU_VCCP-Decoupling



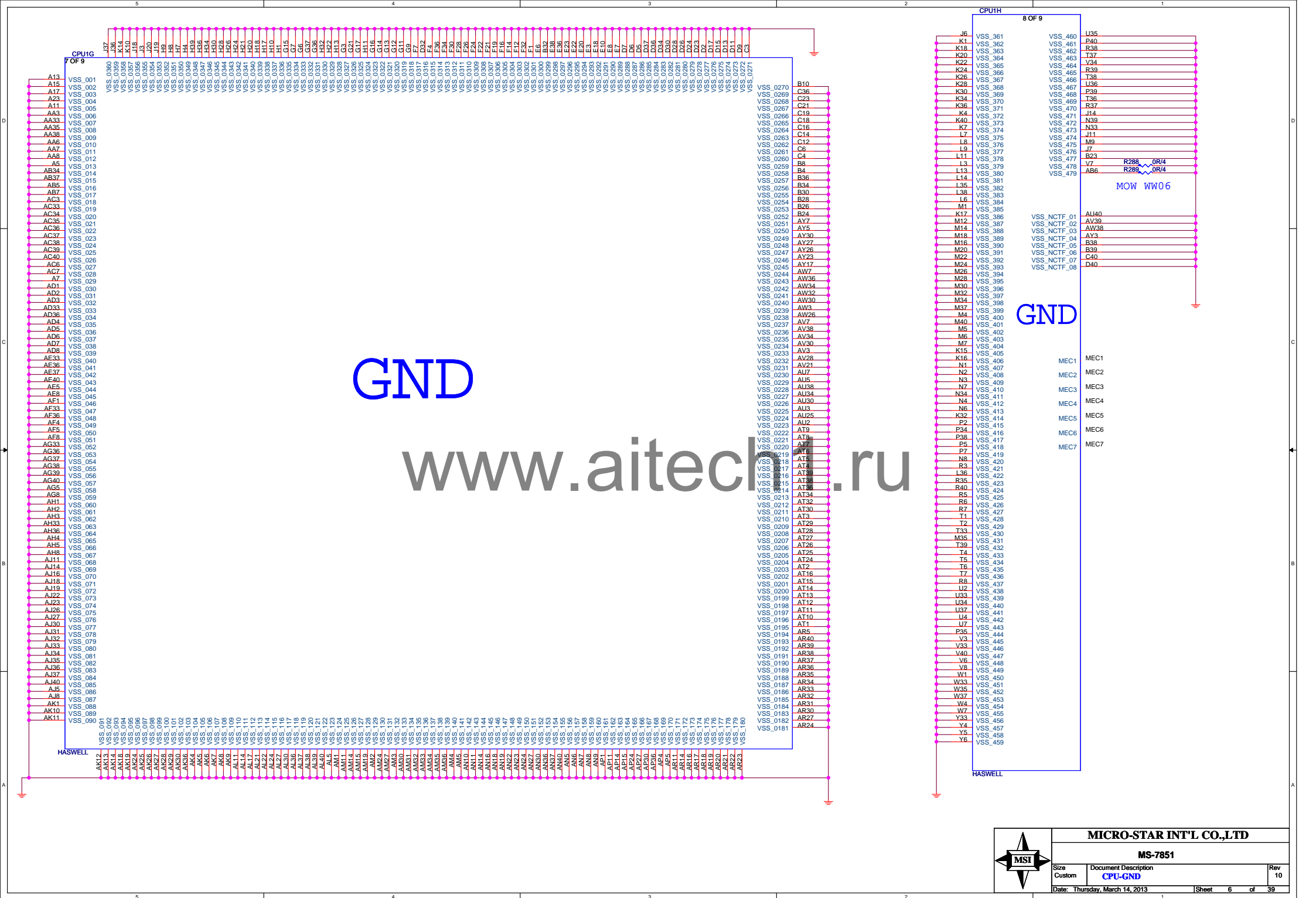
Close to test point



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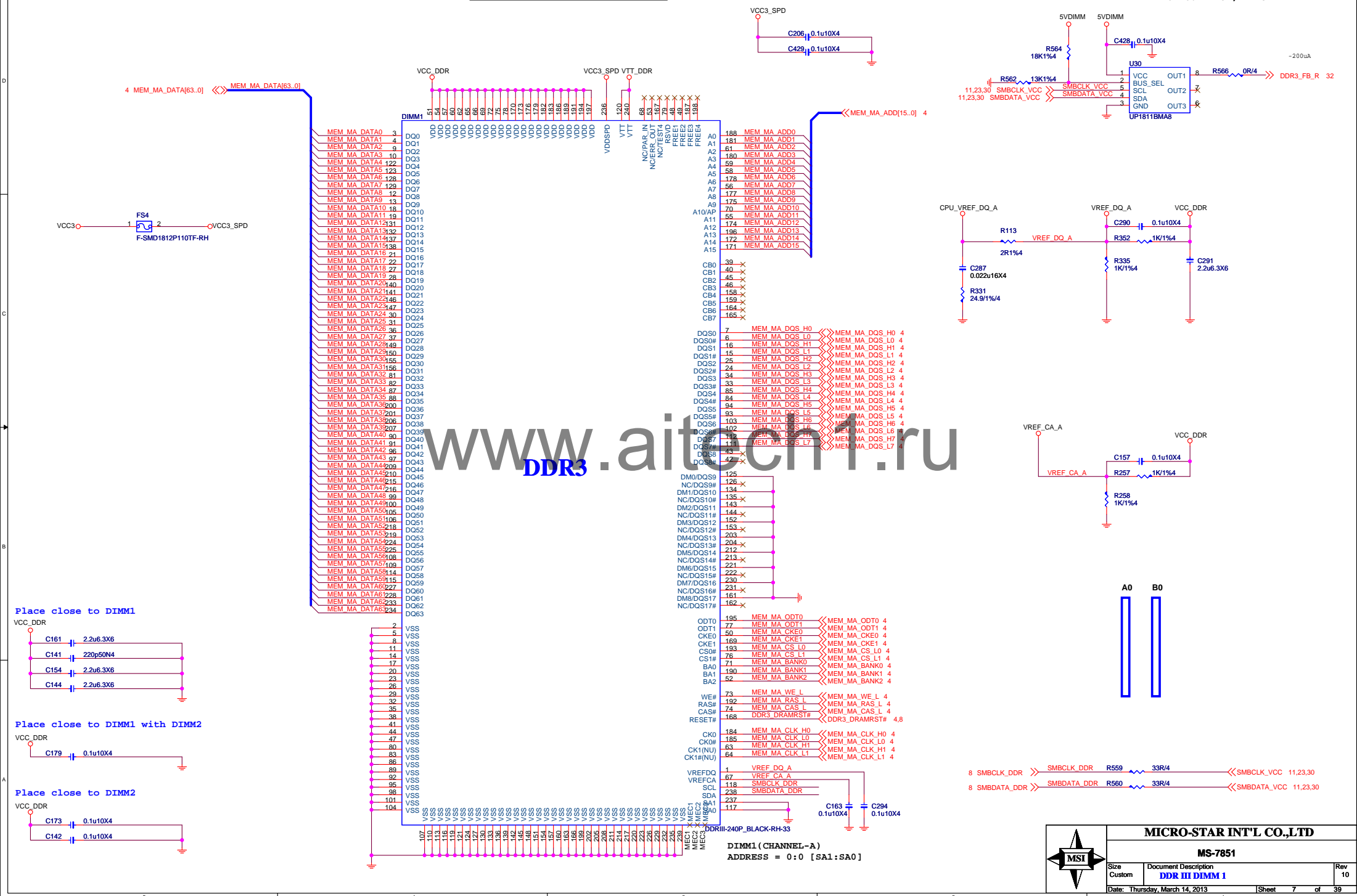
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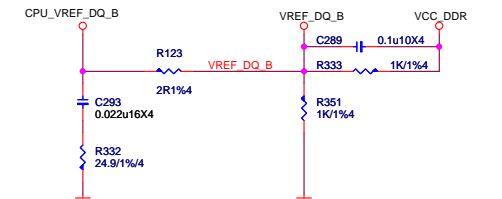
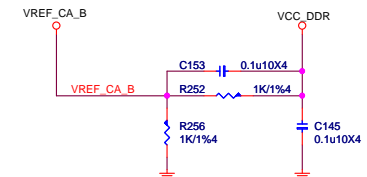
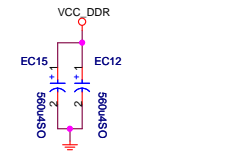
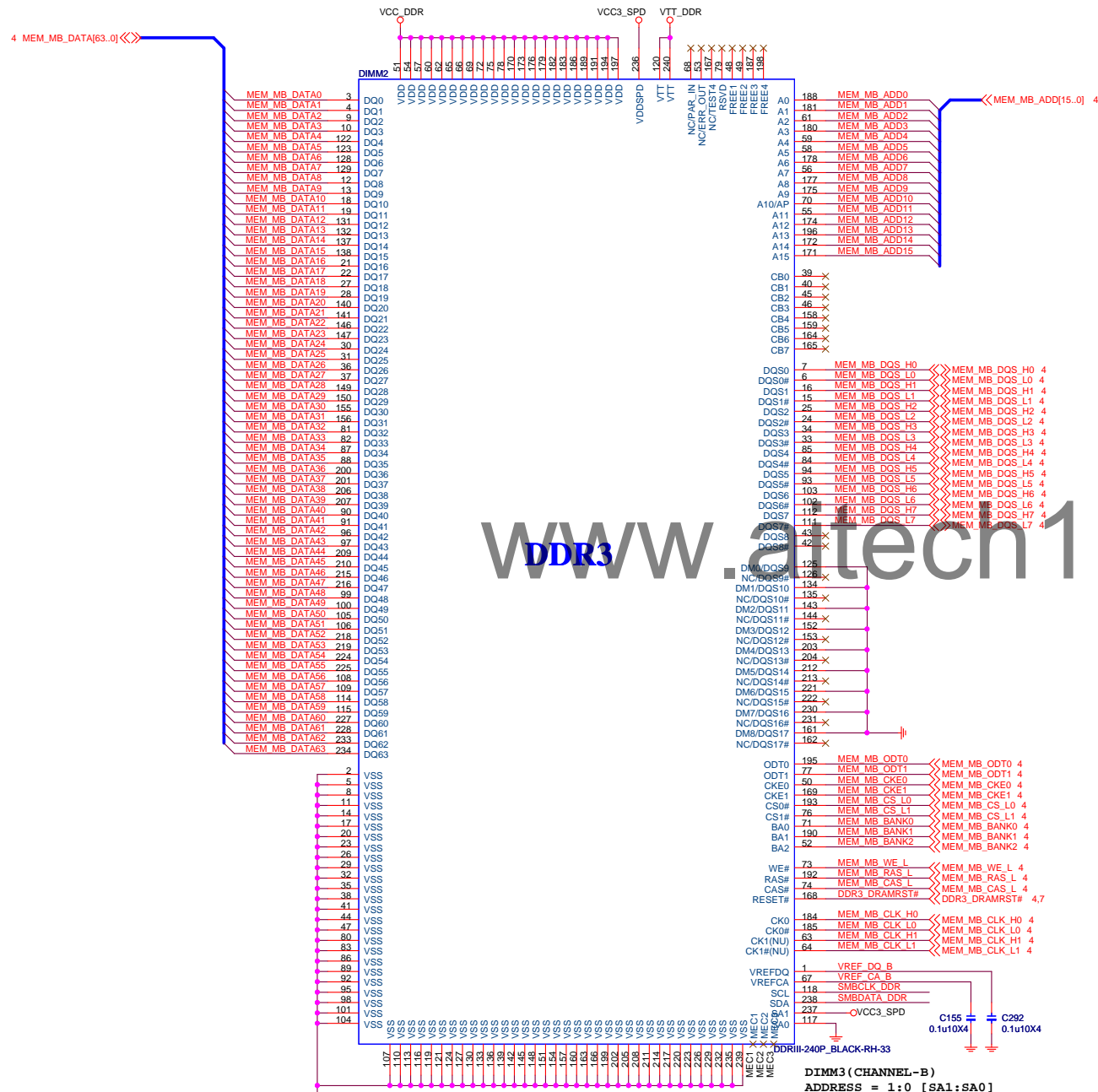
DDRIII DIMM_A0

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



DDRIII DIMM_B0



SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7

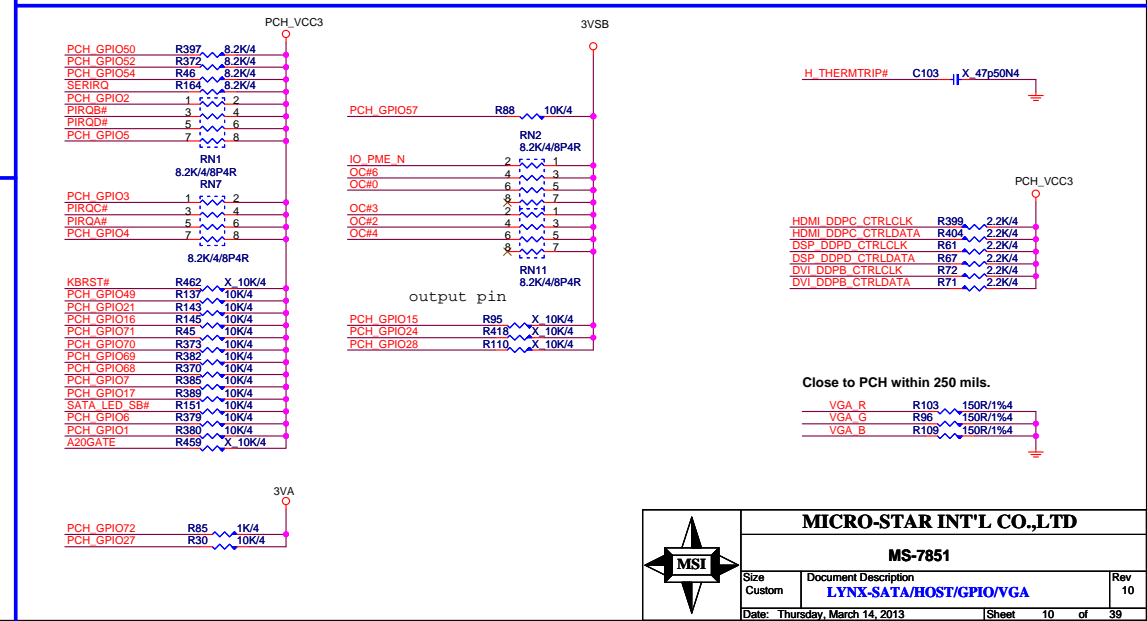
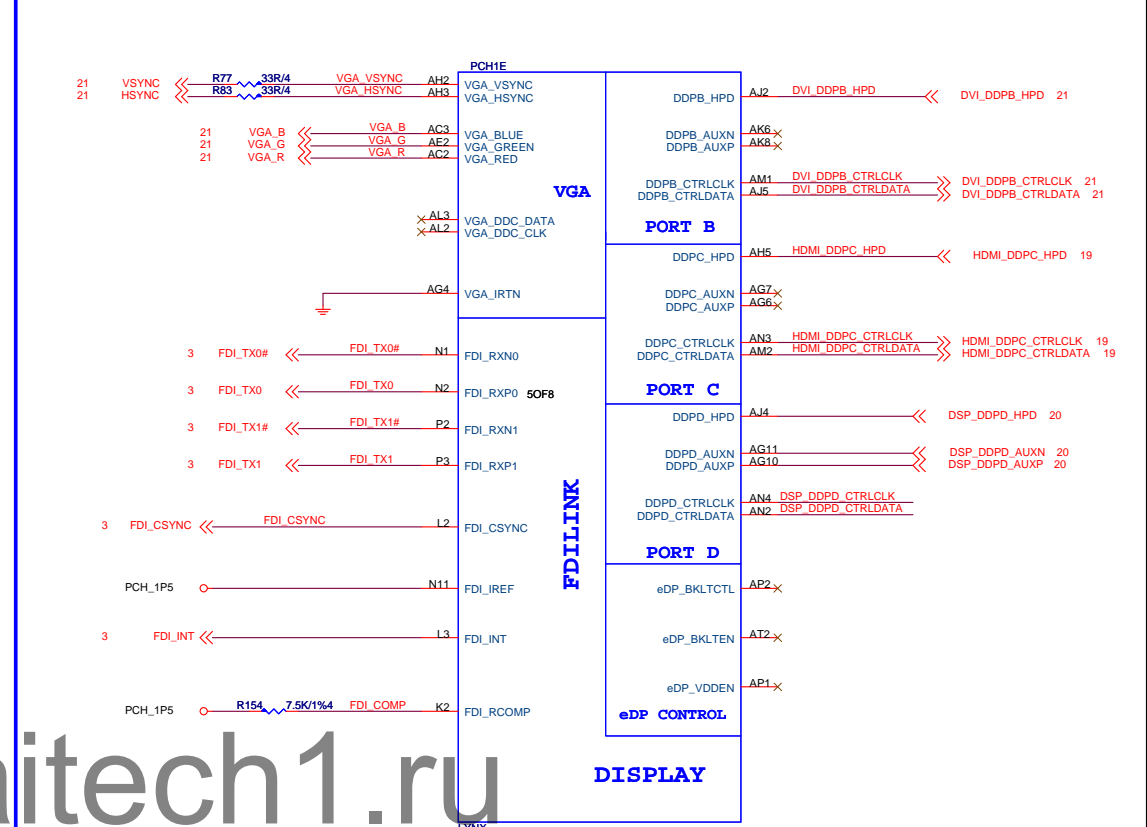
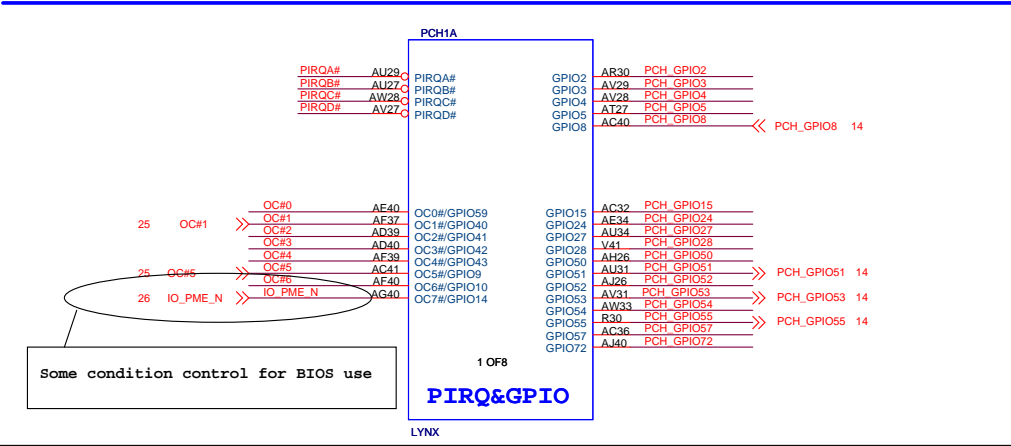
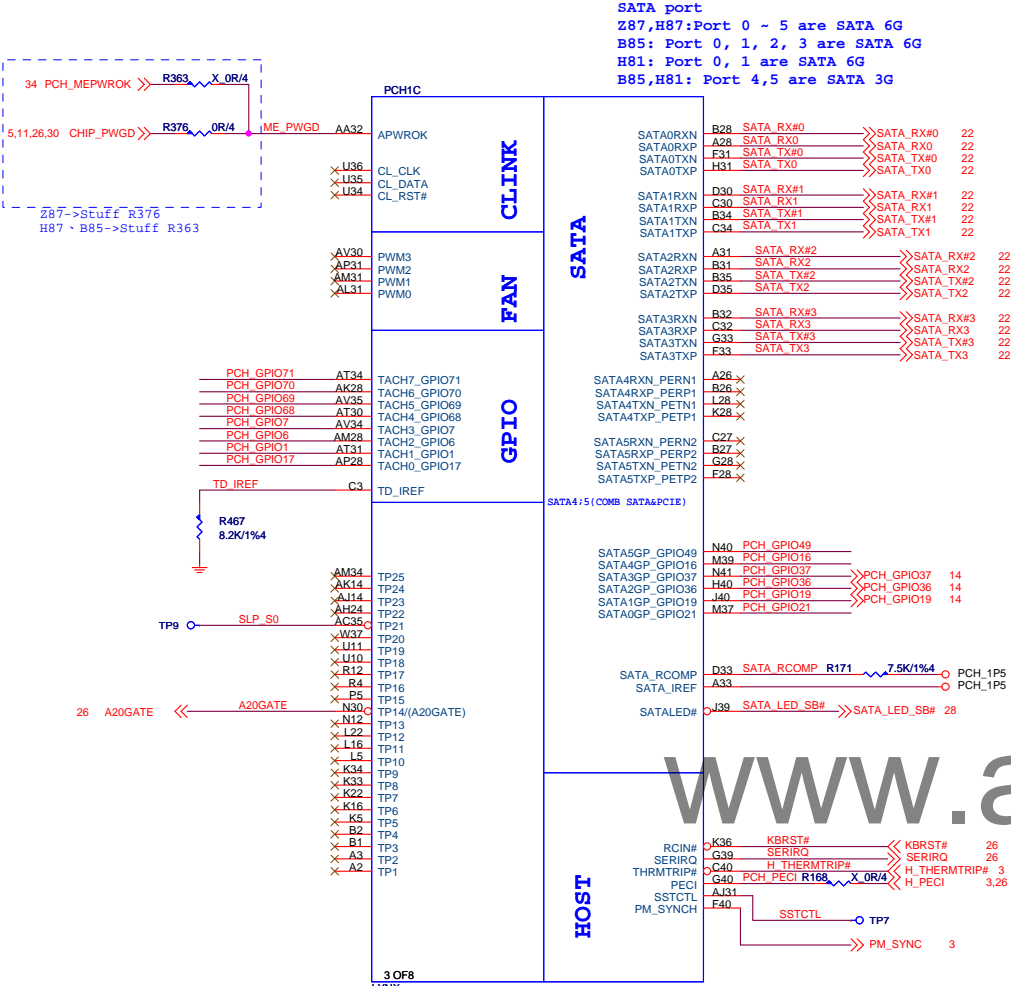


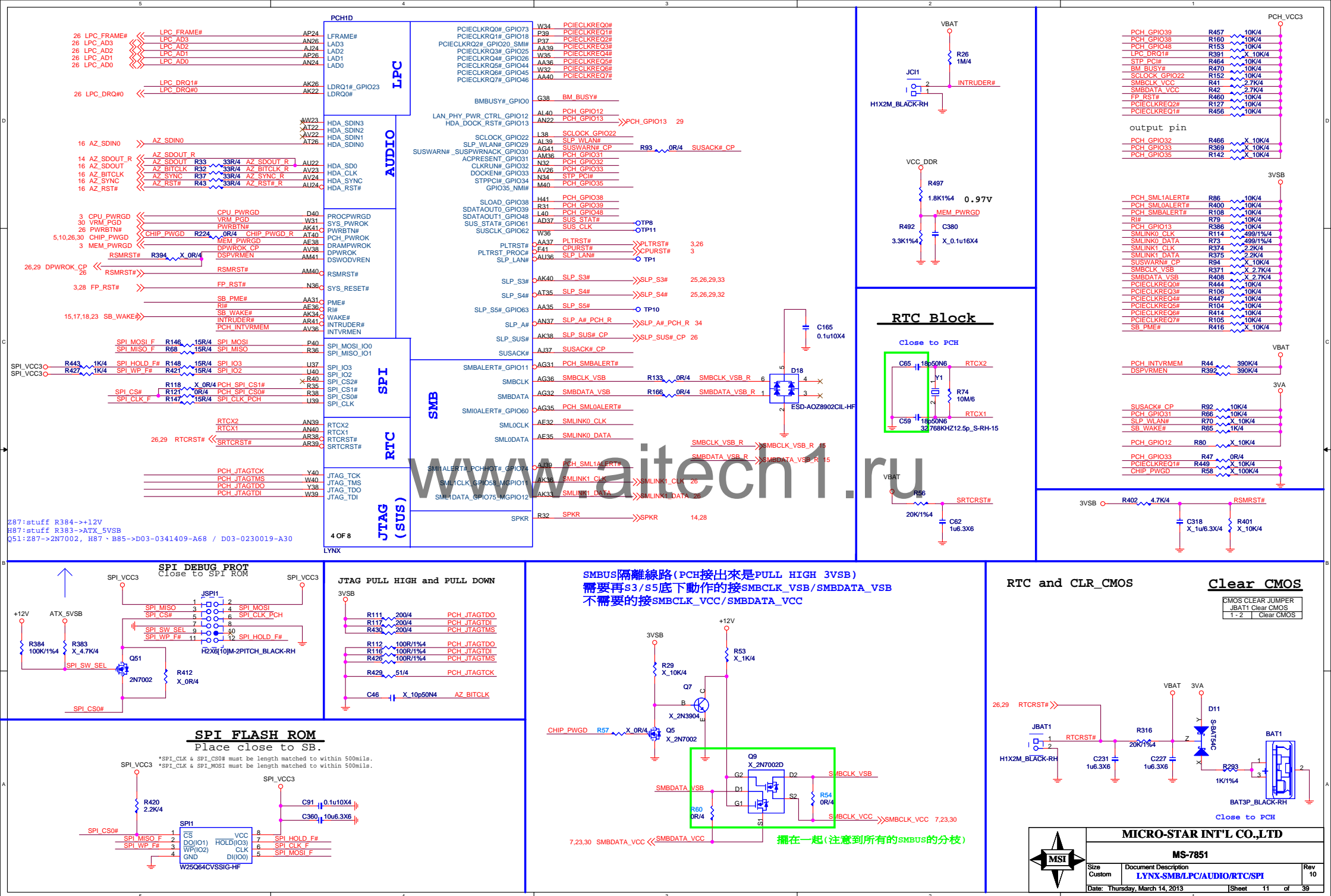
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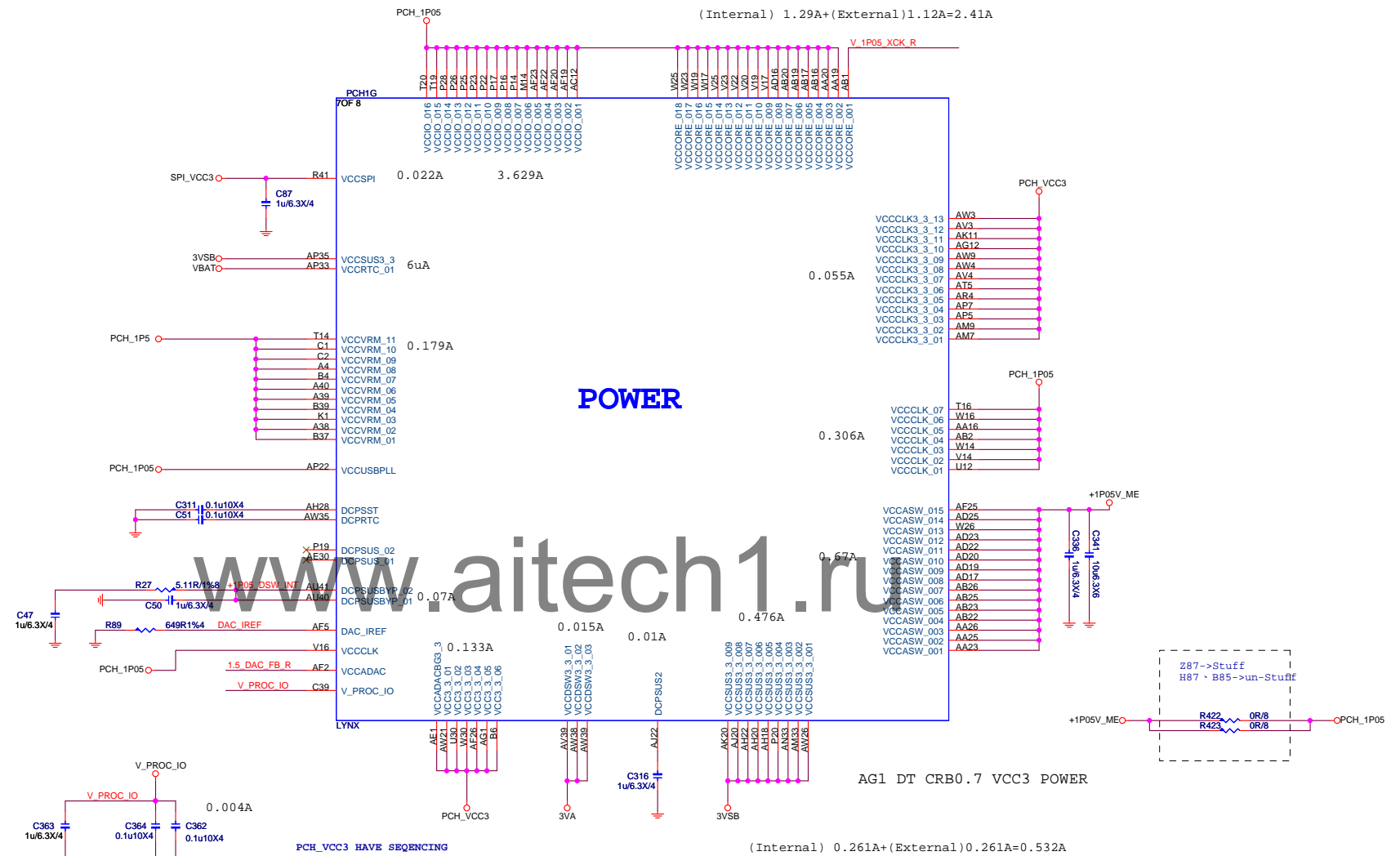
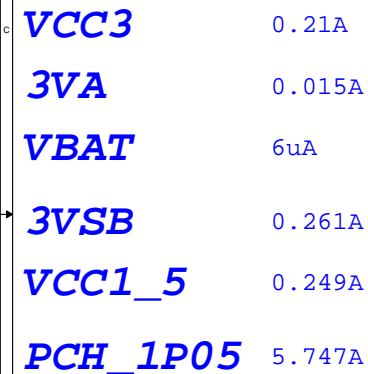
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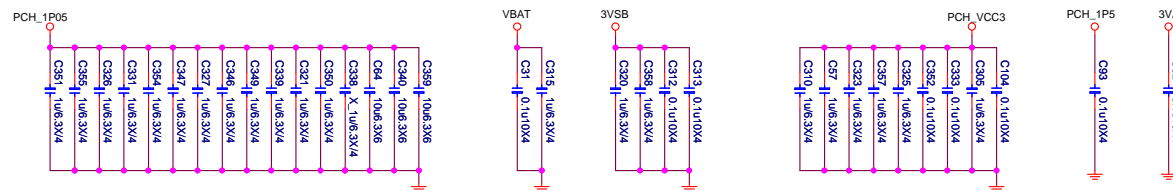
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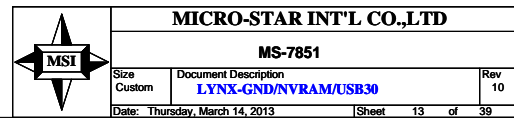
$$(\text{Internal}) \quad 1.29A + (\text{External}) 1.12A = 2.41A$$


PCH decoupling cap



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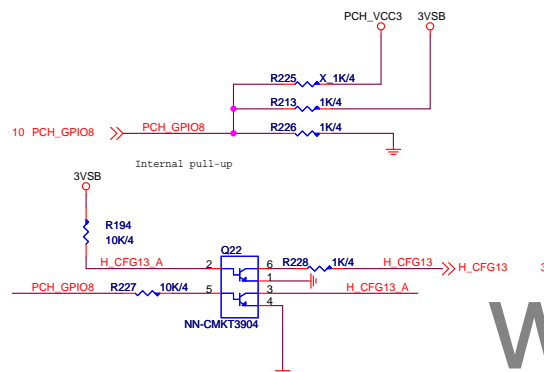
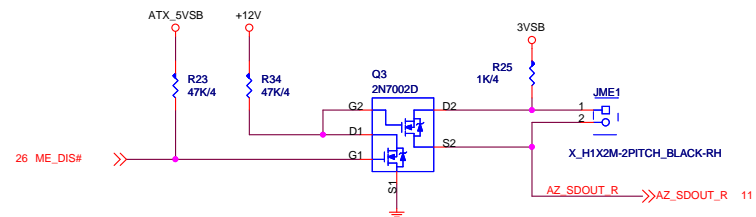


11,28 SPKR << SPKR R448 X 8.2K/4

Internal pull-DOWN

SPKR
Default Mode:
Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.



10 PCH_GPIO55 >> PCH_GPIO55 R415 X 4.7K/4

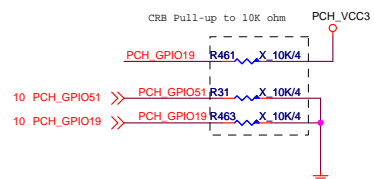
Internal pull-up

GPIO55
Default Mode:
Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.

10 PCH_GPIO53 >> PCH_GPIO53 R36 X 1K/4

GPIO53
Connect to ground with 1k Ohm pull-down resistor.



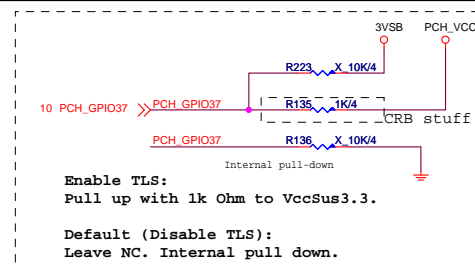
Default (SPI):
Left both SATA1GP/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:
Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:
Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.

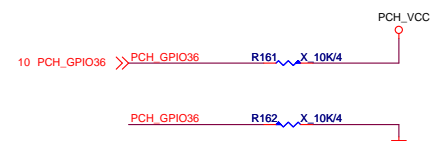
BOOT DEVICE	GPIO51	GPIO19
LPC	0	0
SPI	1	1

Default

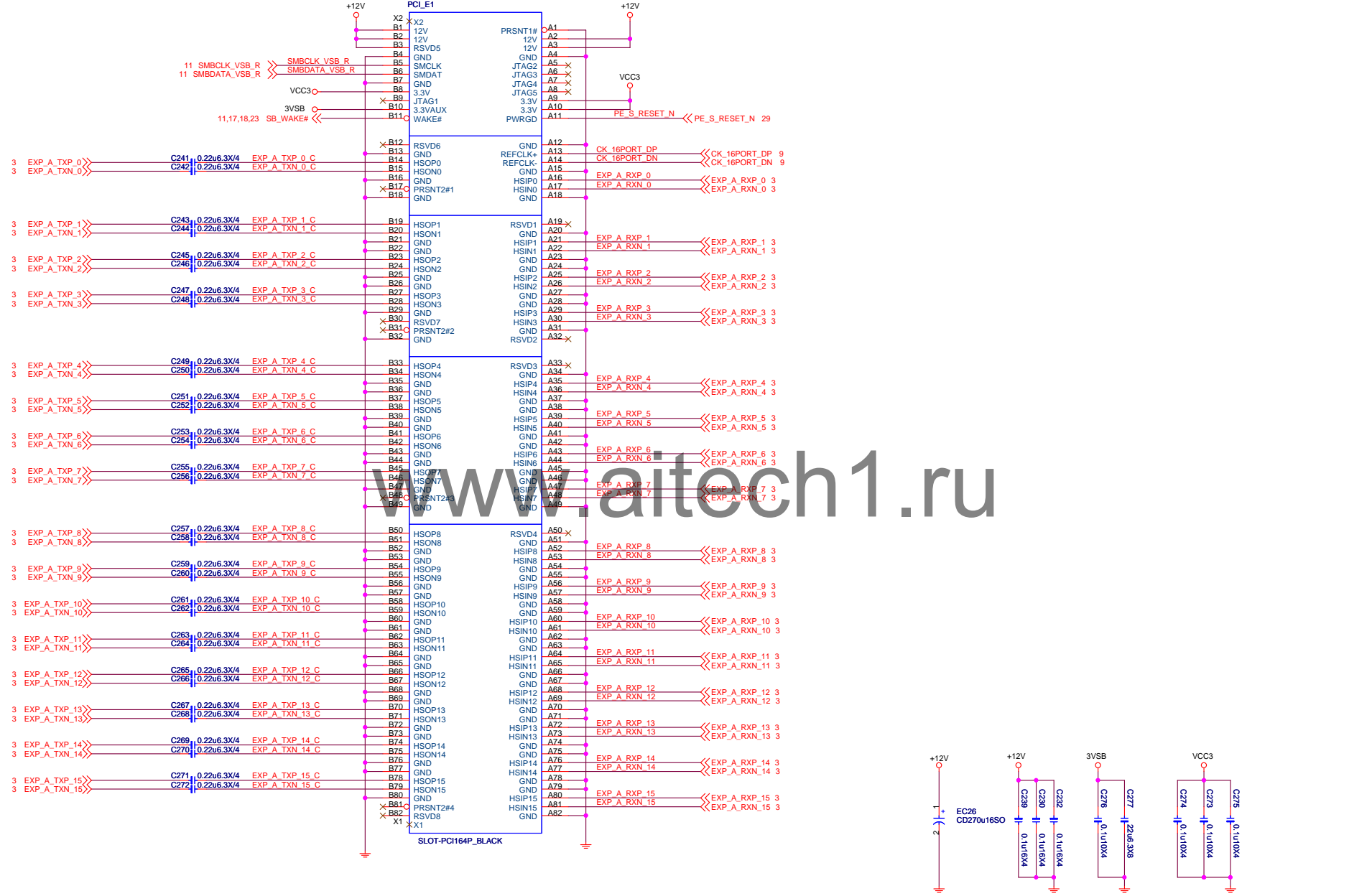


Enable TLS:
Pull up with 1k Ohm to VccSus3.3.

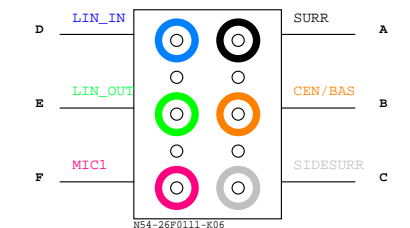
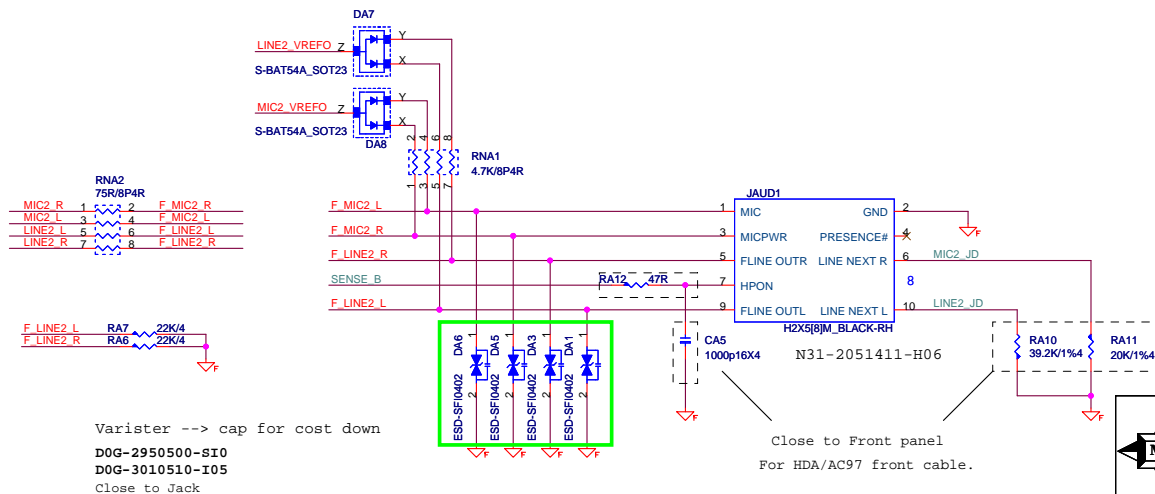
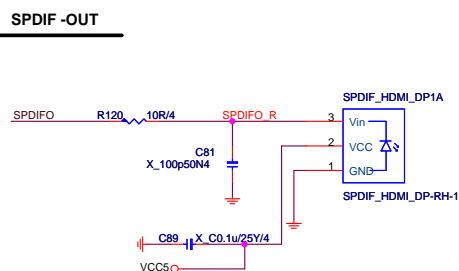
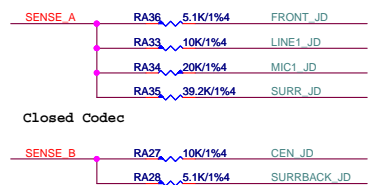
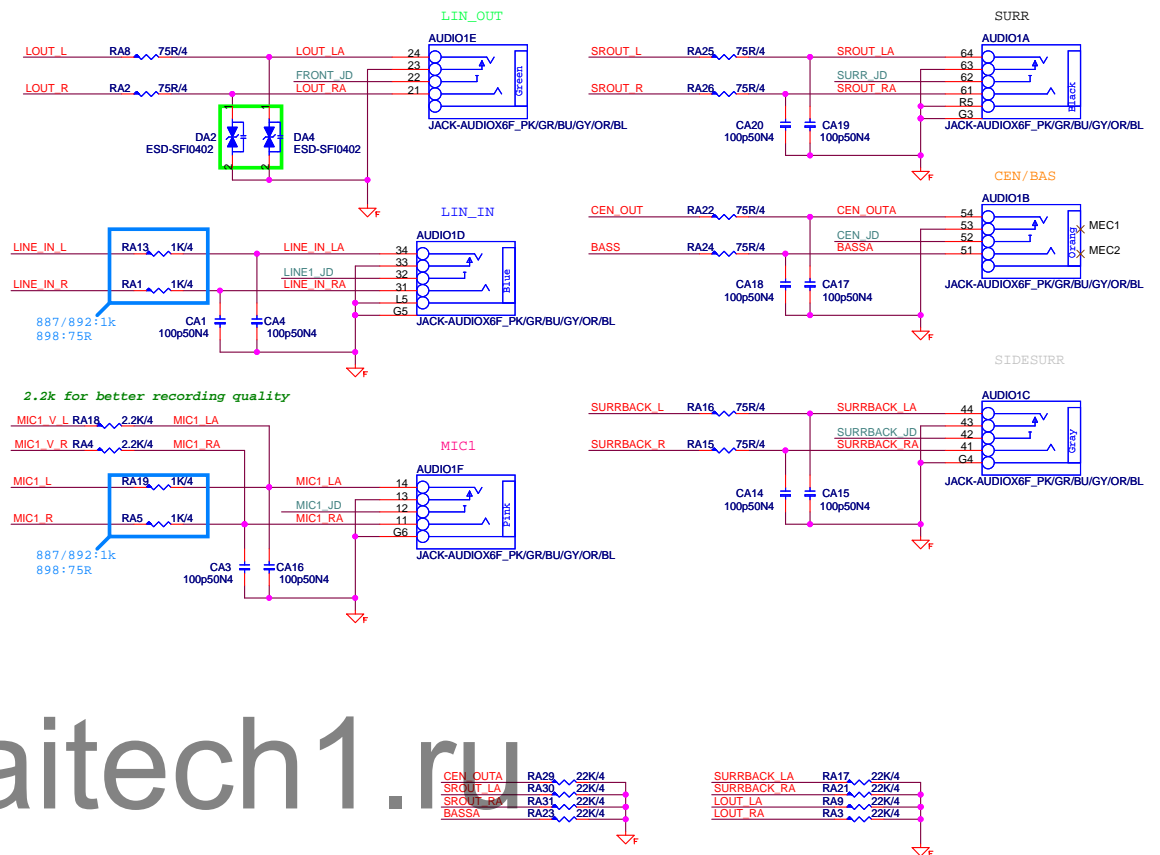
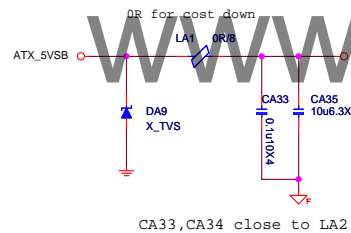
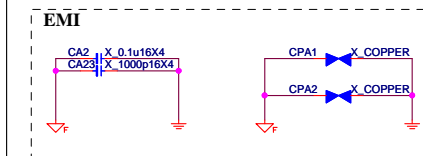
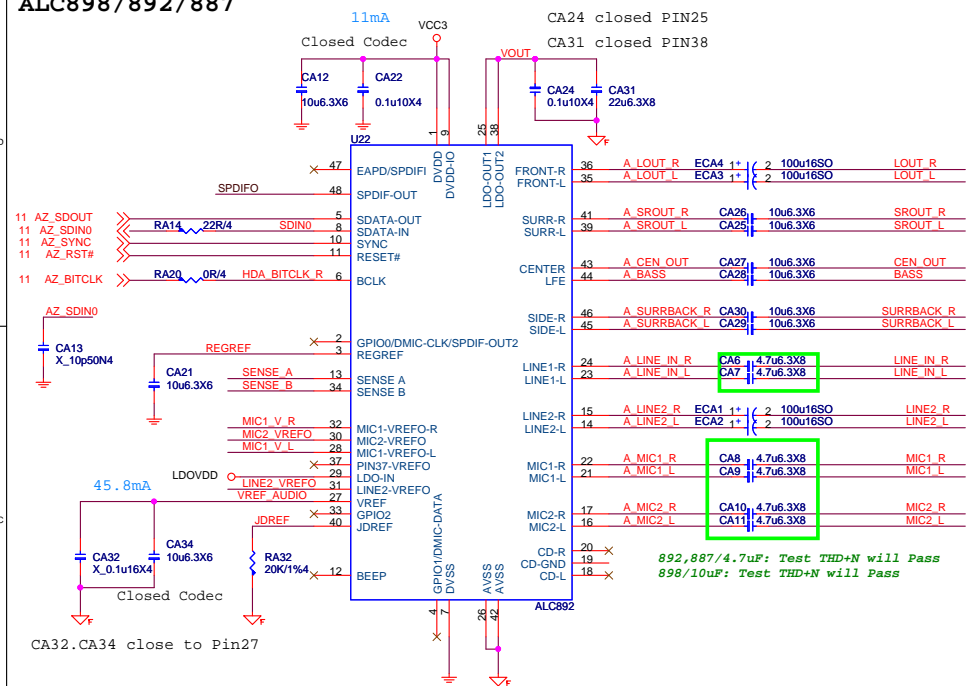
Default (Disable TLS):
Leave NC. Internal pull down.



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Type A:
ALC898/892/887



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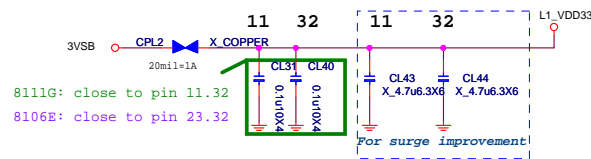
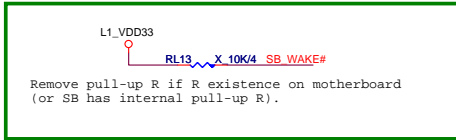
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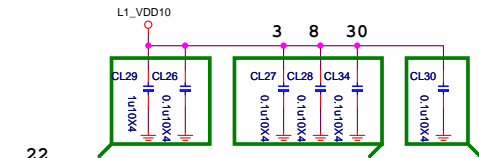
RTL8111G Giga LAN

RTL8106E 10/100M LAN

LAN Connector

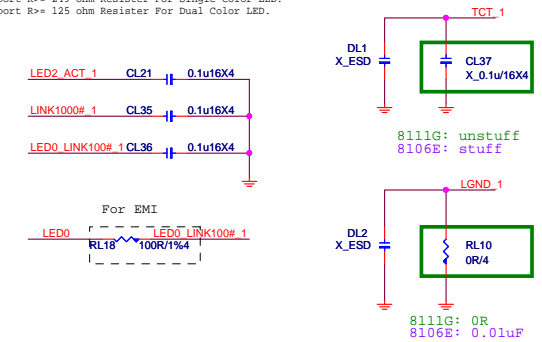
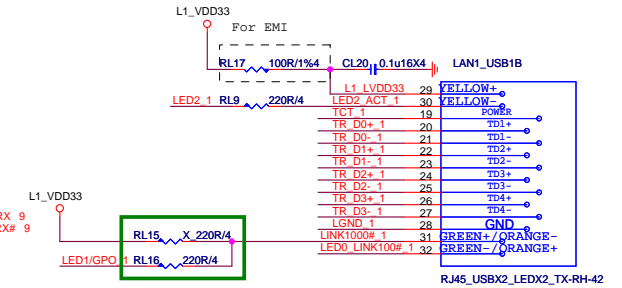
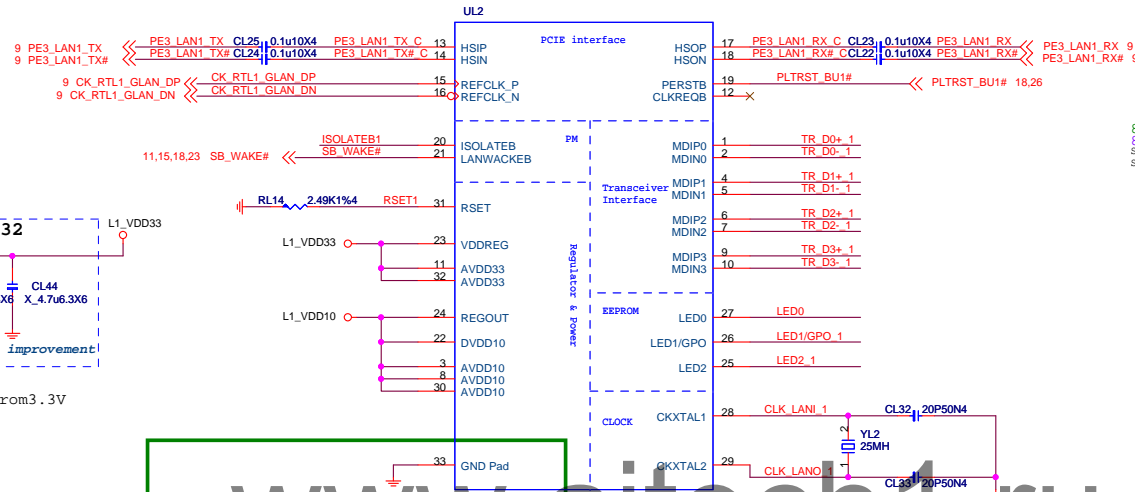


Icc33 average operating supply current from 3.3V
At 1Gbps with heavy network traffic 70mA

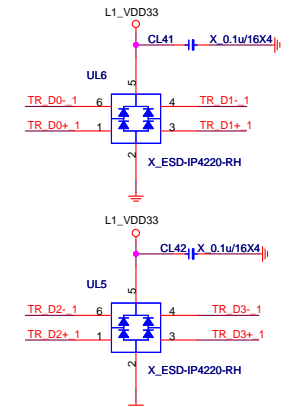


8111G: close to pin 22 8111G: close to pin 3.8.30 8111G: LDO mode close to pin 24
8106E: close to pin 30 8106E: close to pin 8.30 8106E: unstuff

30 Icc10 average operating supply current from 1.0V
At 1Gbps with heavy network traffic 300mA

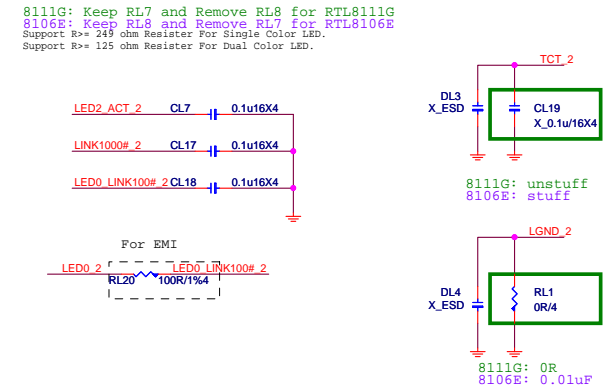
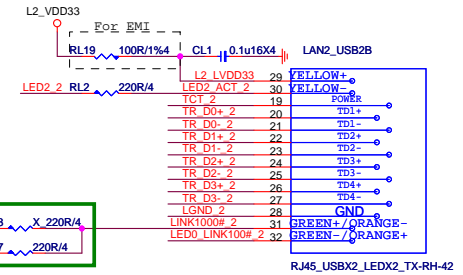


Reserve ESD Protect



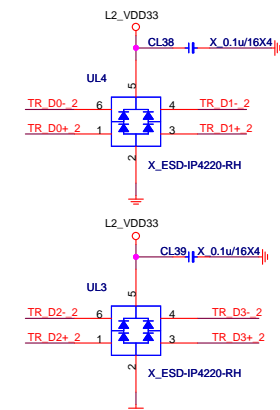
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MS-7851			
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LAN Connector



For EMI

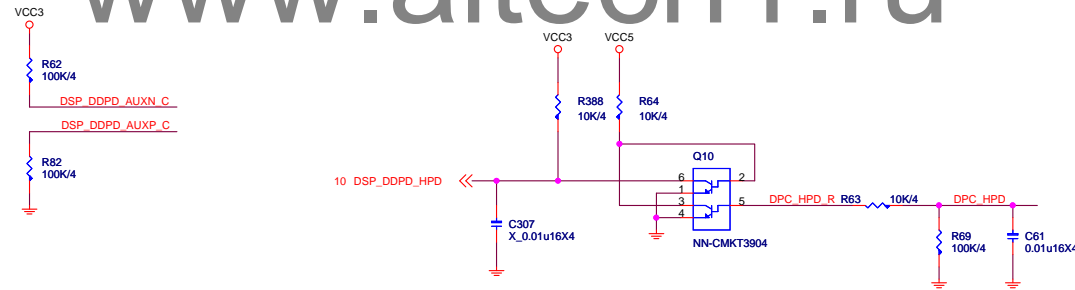
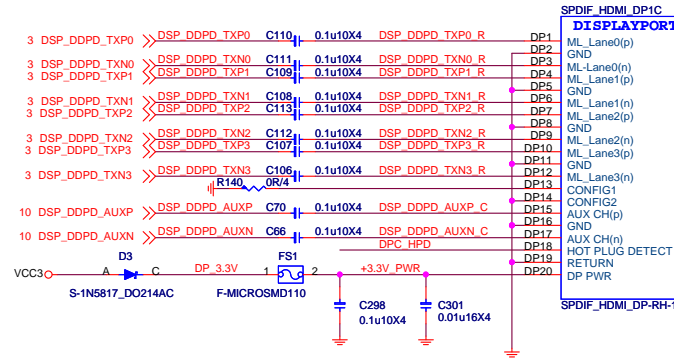
LED0 2 [---] LED0 LINK100#
RL20 100R/1%4



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DP



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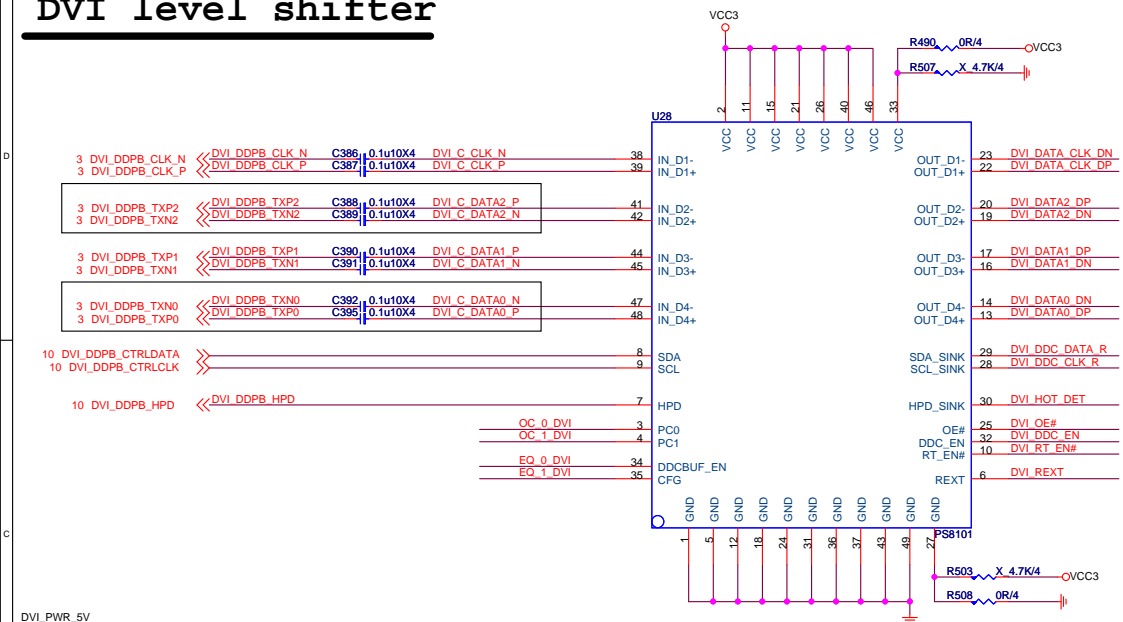


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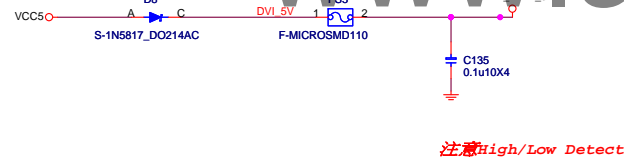
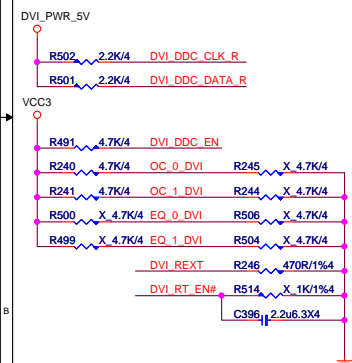
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DVI level shifter



PERICOM料號:B0B-411LS2C-P22.

PARADE料號:B0B-081010C-P97.



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

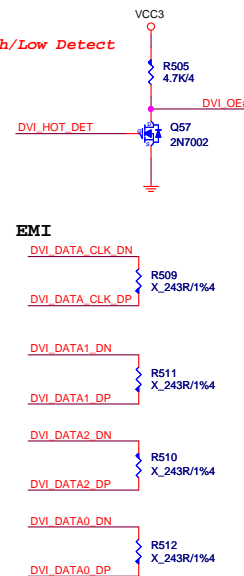
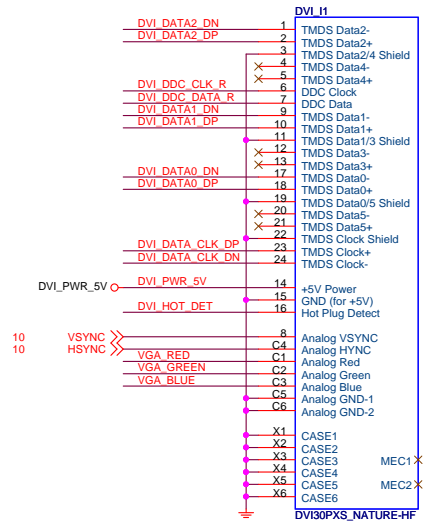
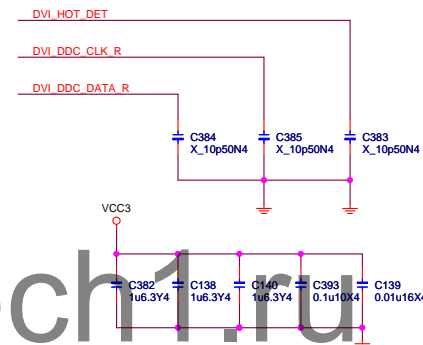
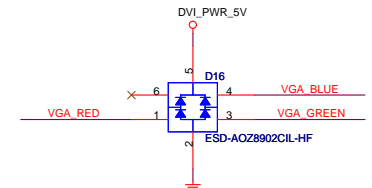
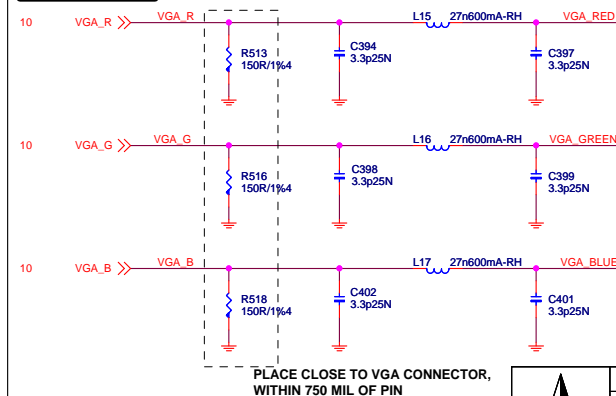


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIb_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMIb_CTRL_DATA		



D-Sub



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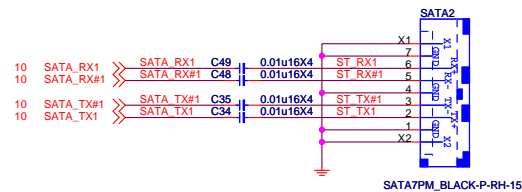
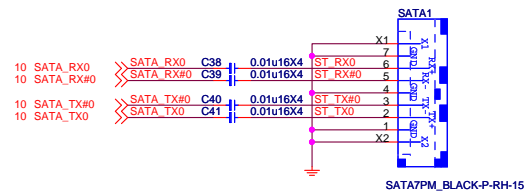
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SATA port
Z87,H87:Port 0 ~ 5 are SATA 6G
B85: Port 0, 1, 2, 3 are SATA 6G
H81: Port 0, 1 are SATA 6G
B85,H81: Port 4,5 are SATA 3G

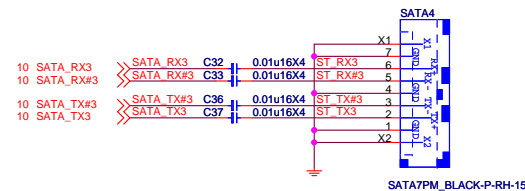
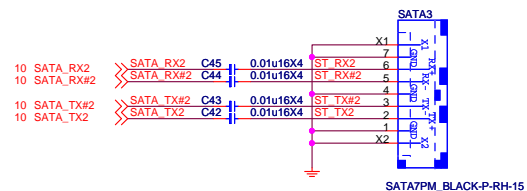
SATA 6G PORT 0,1

3.0 BLACK



SATA 6G PORT 2,3

3.0 BLACK



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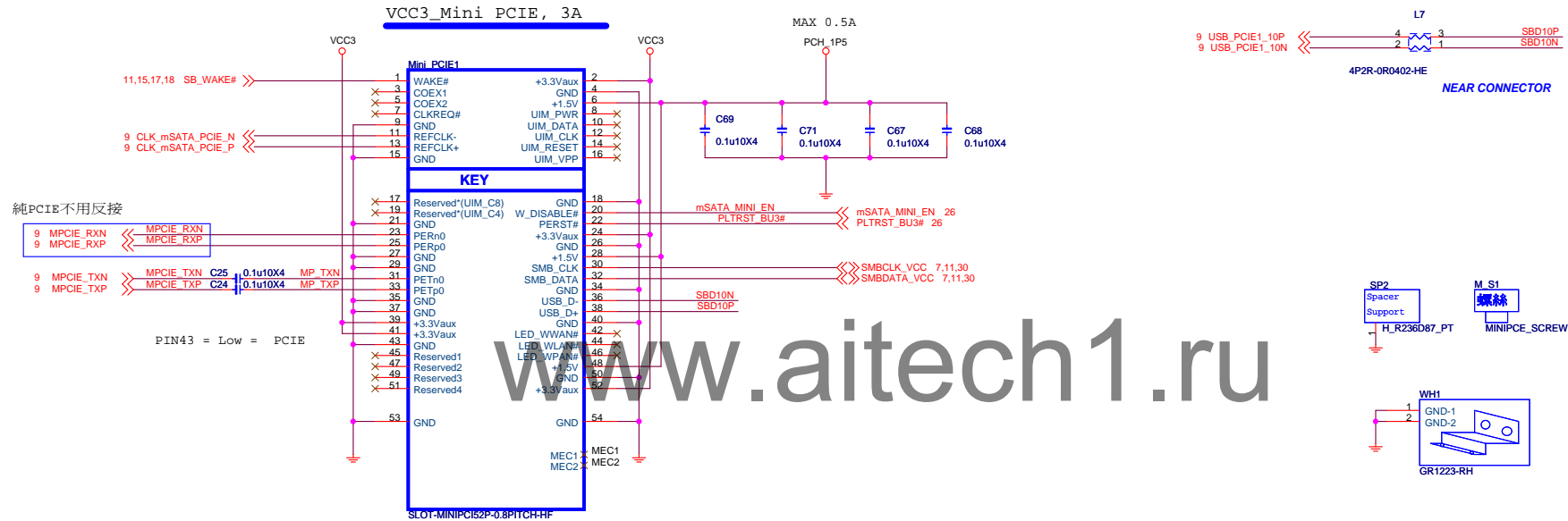


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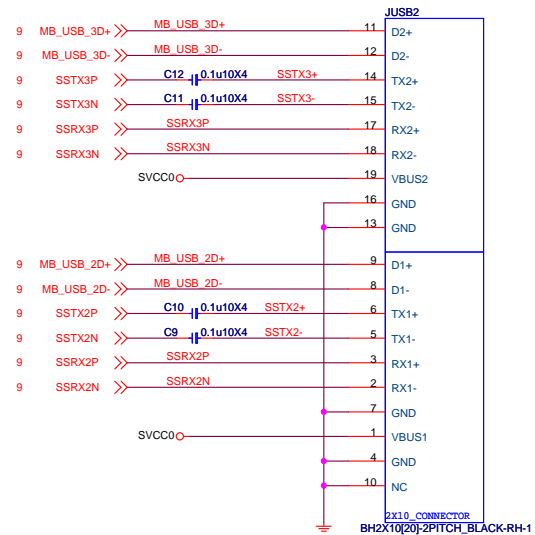
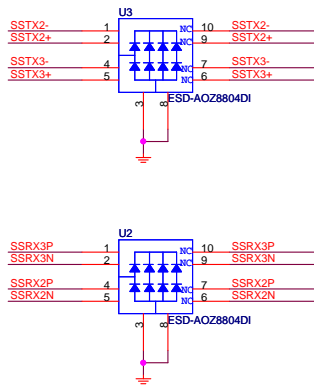
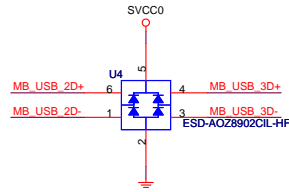
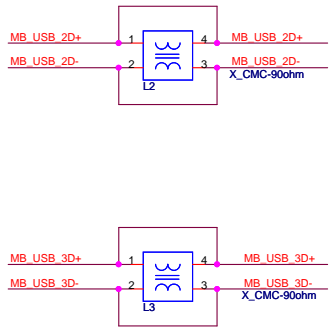
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Custom	SATA Connector	10
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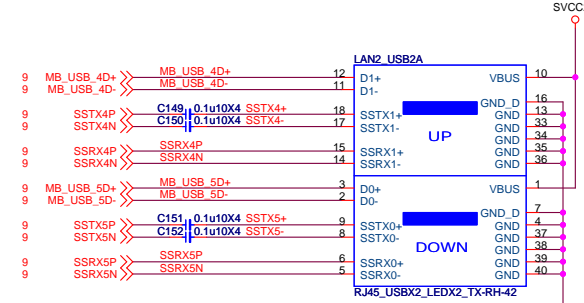
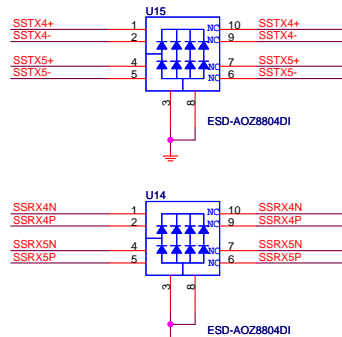
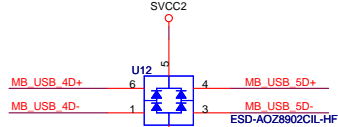
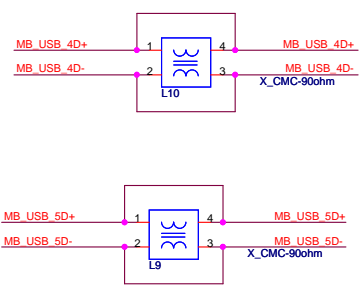
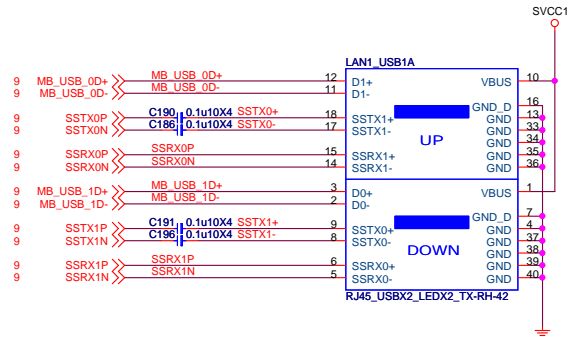
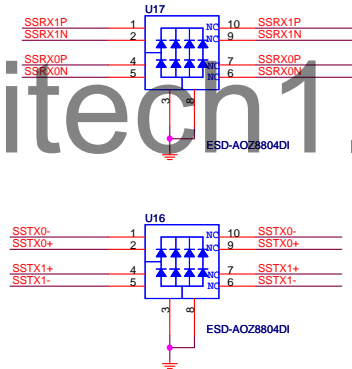
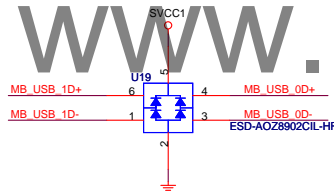
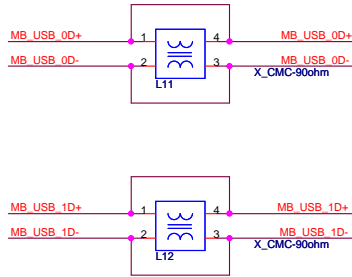
Mini PCIE SHORT CARD

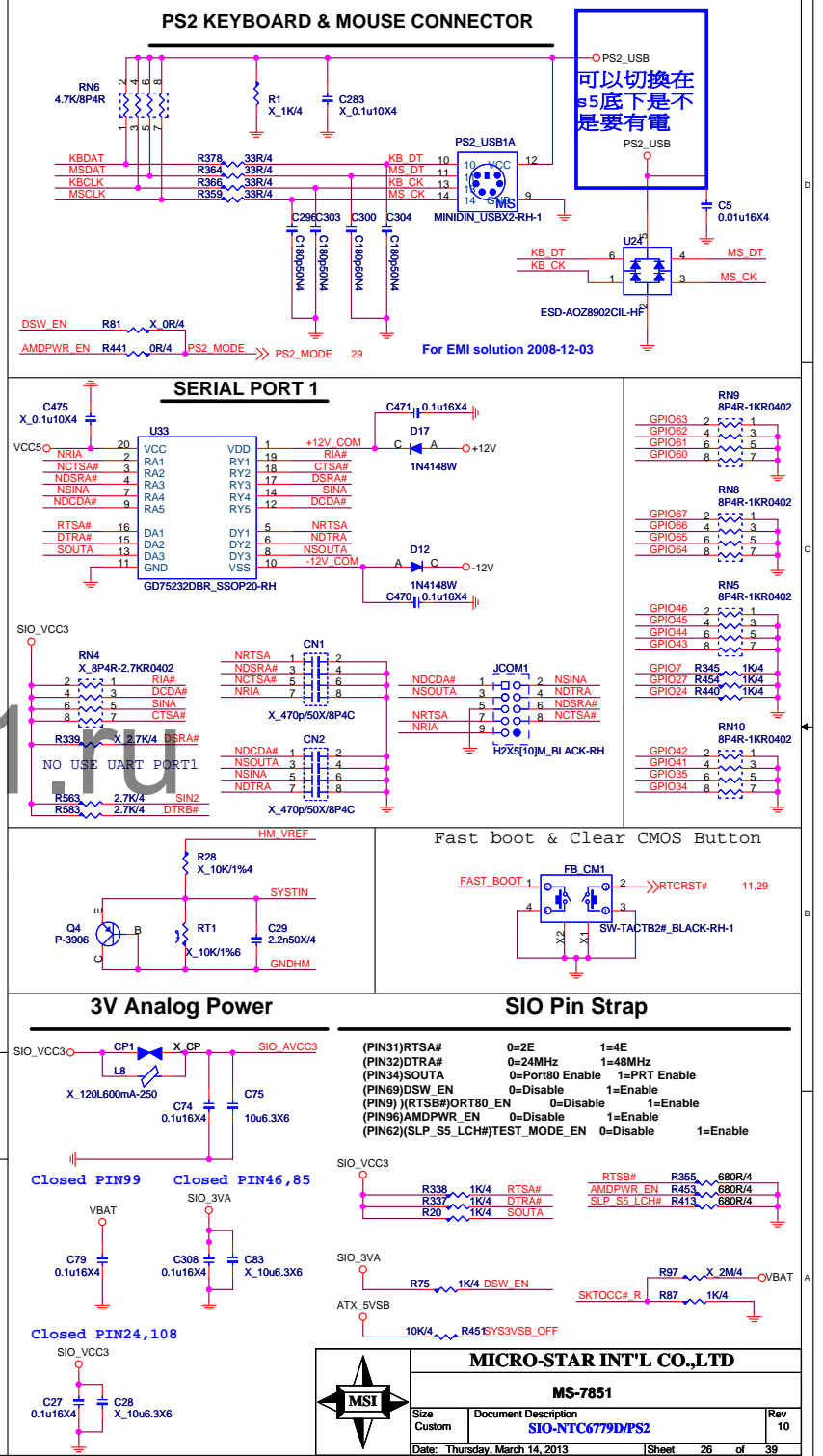
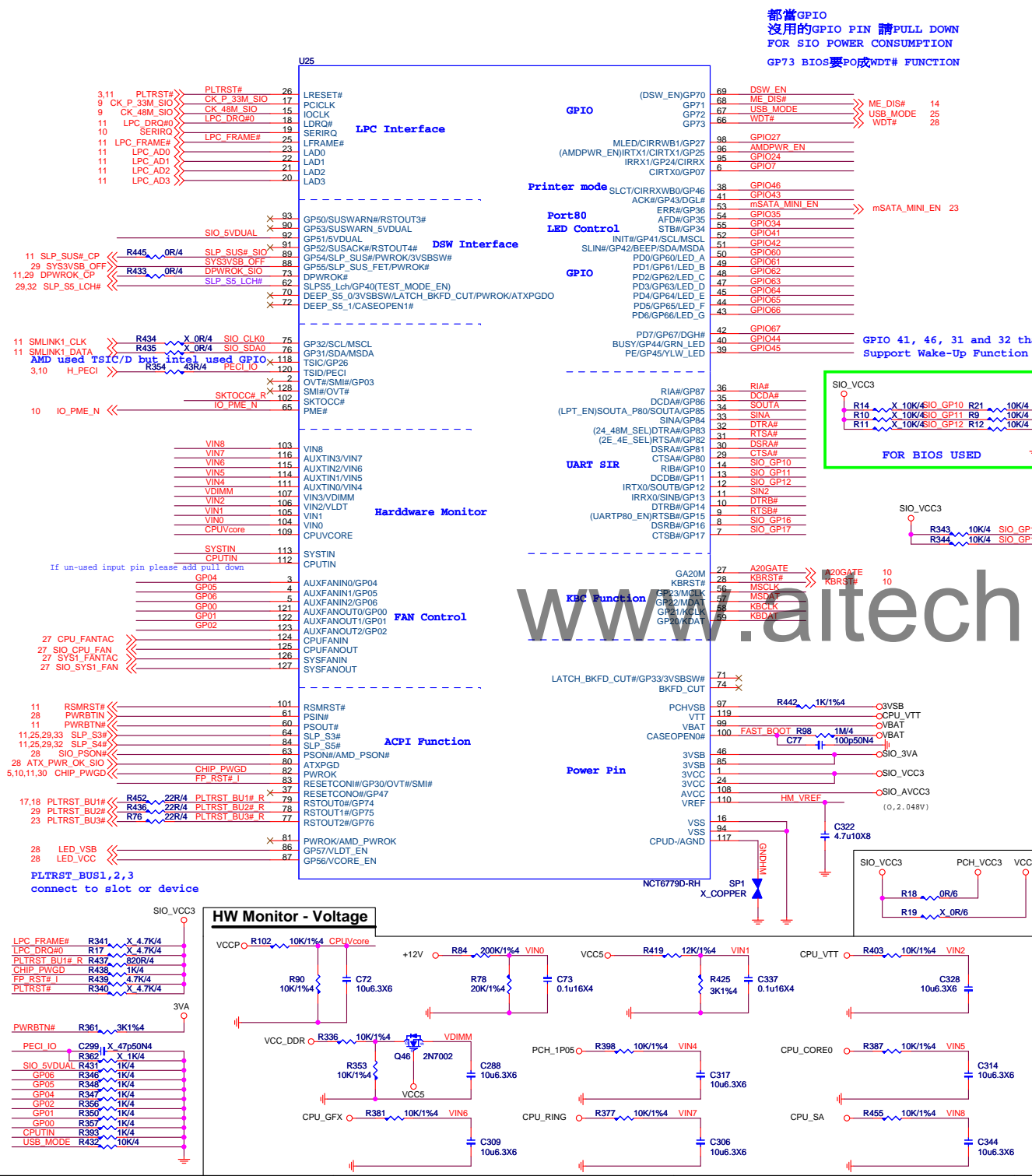


Front USB 3.0



Rear USB 3.0

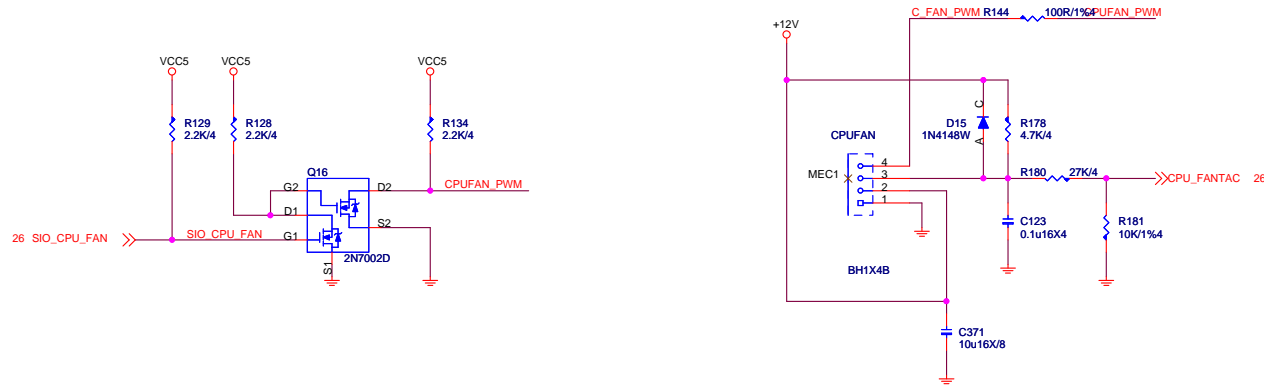




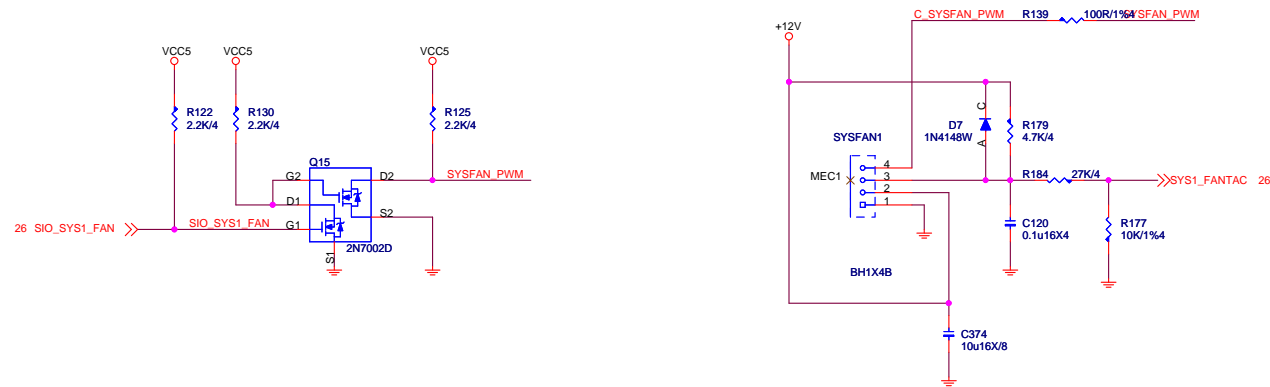
MICRO-STAR INT'L CO.,LTD		
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FAN-COUNTROL CIRCUIT

CPUFAN TYPE E



SYSTEM FAN1 (PWM MODE)



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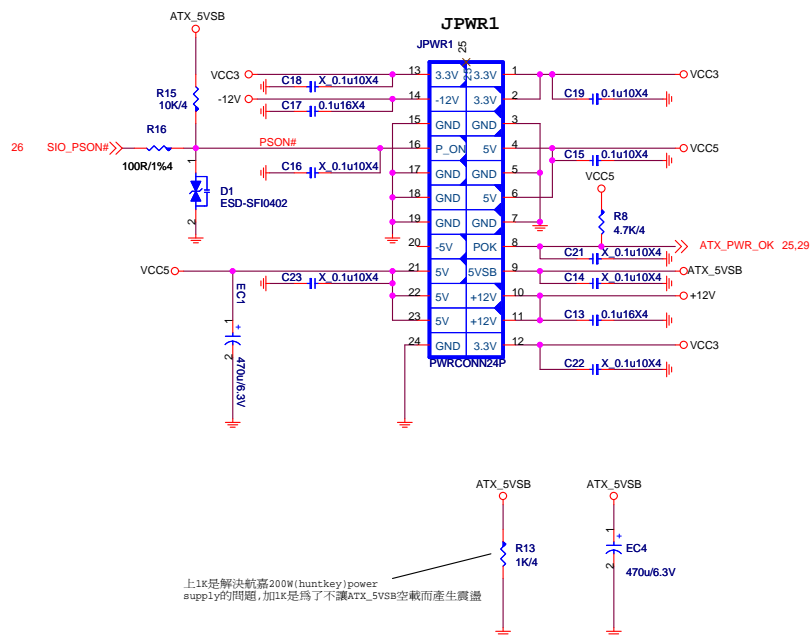


MICRO-STAR INT'L CO.,LTD

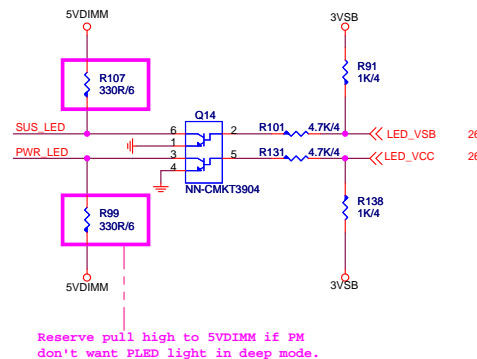
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Custom	FAN Control	10
Date:	Thursday, March 14, 2013	Sheet 27 of 39

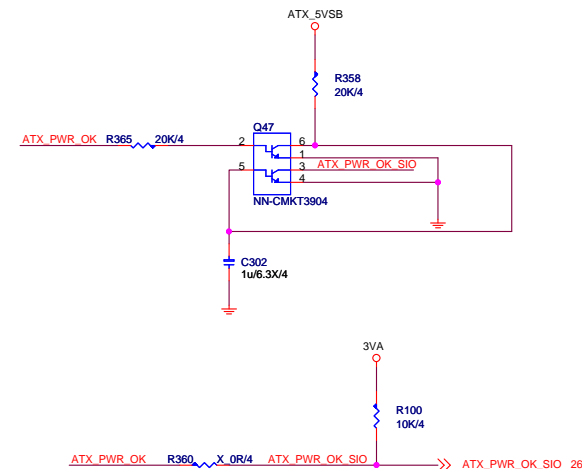
ATX POWER CONNECTOR



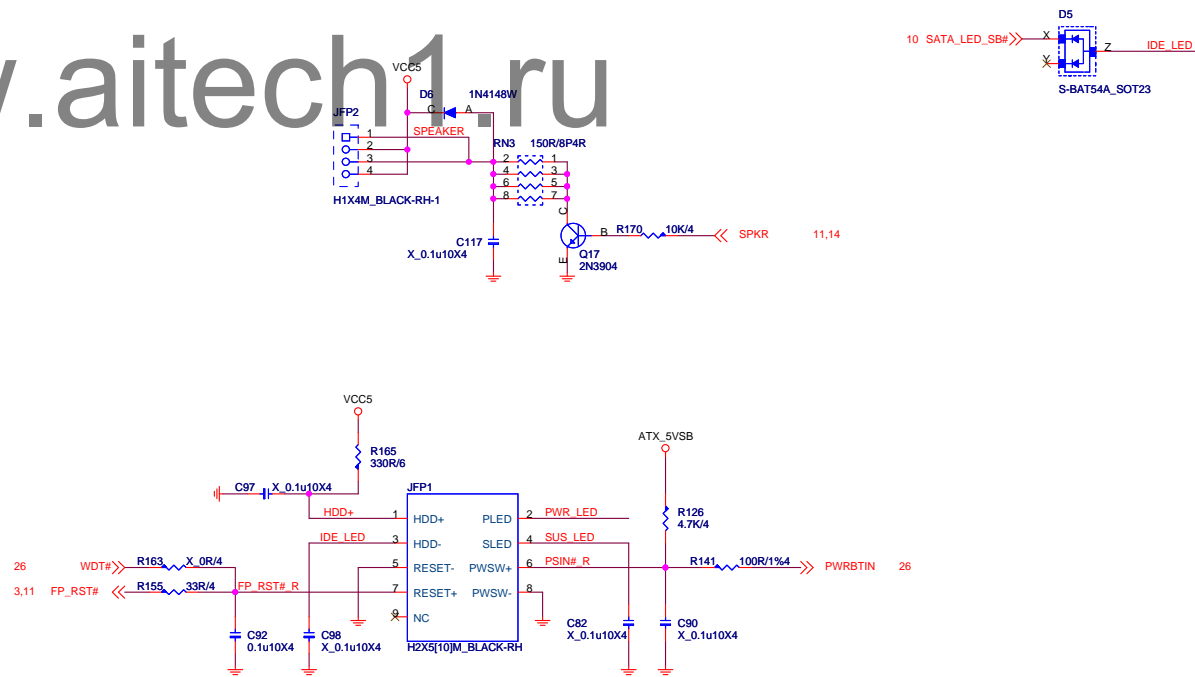
LED (for Fintek NTC6779D)



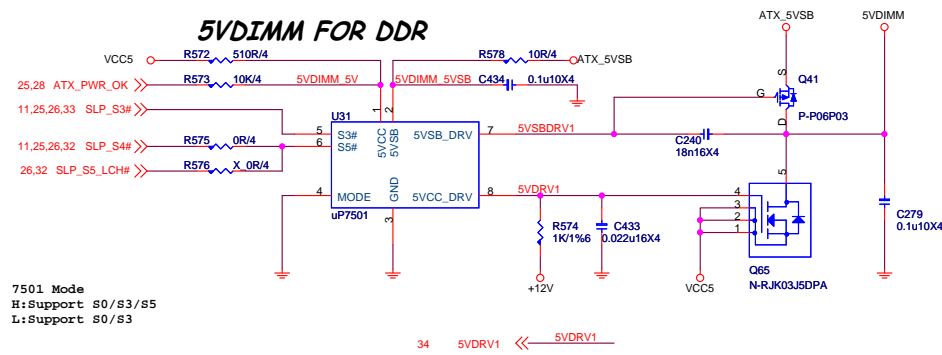
5VCC leakage from ATXPGD



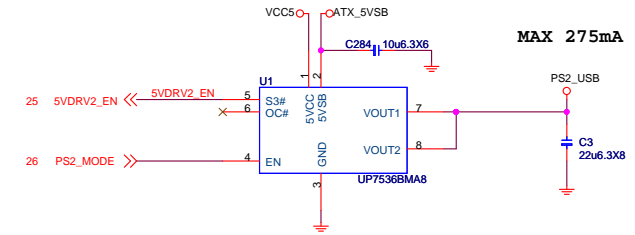
FRONT PANNEL



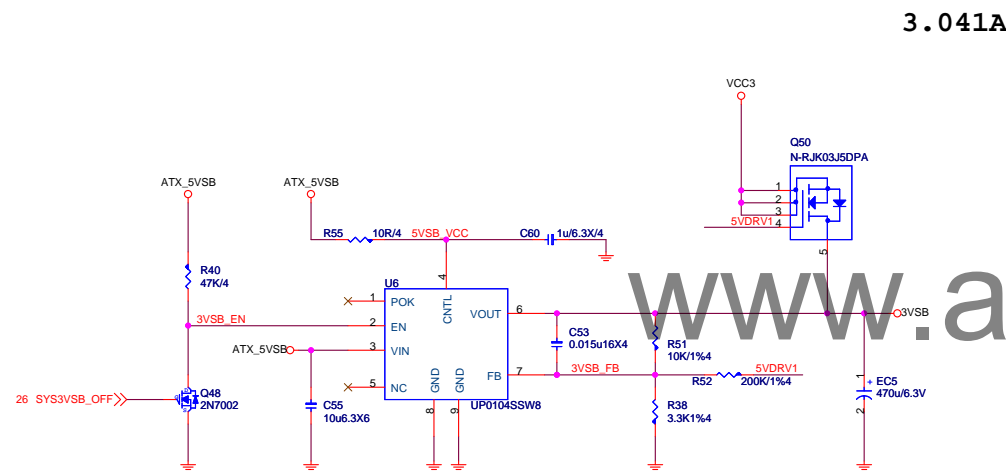
5VDIMM FOR DDR



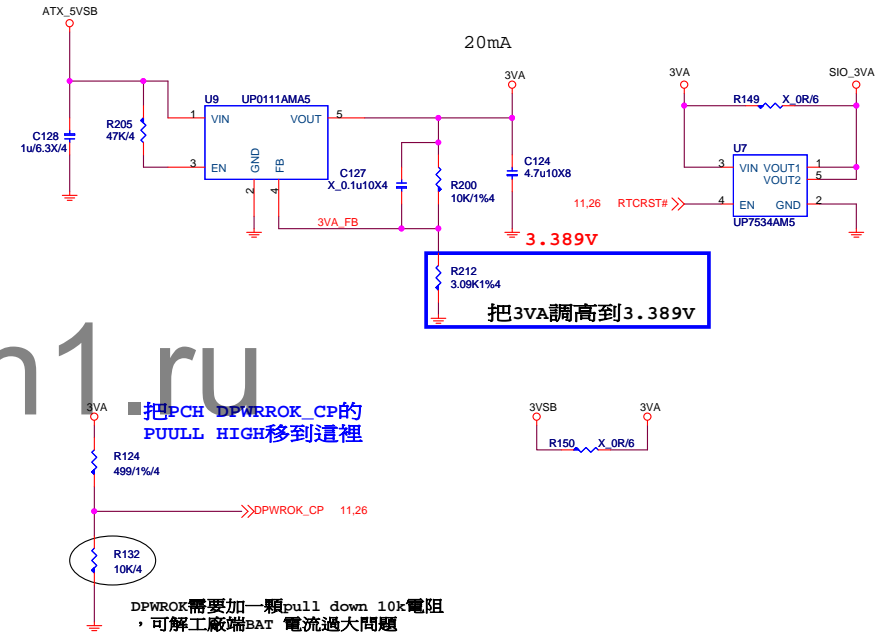
PS2 Power



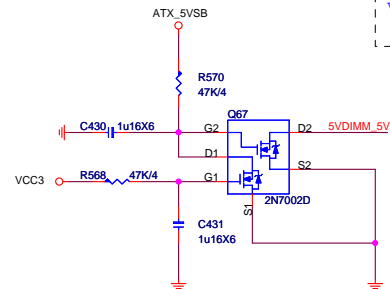
3VSB



3VA

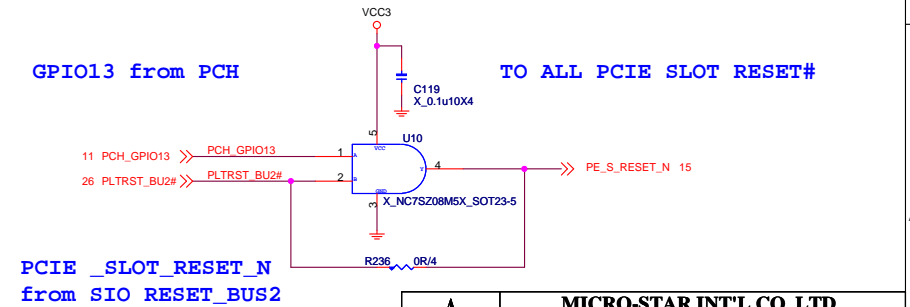


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

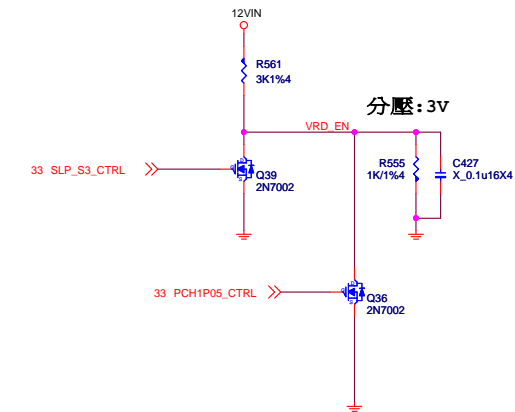
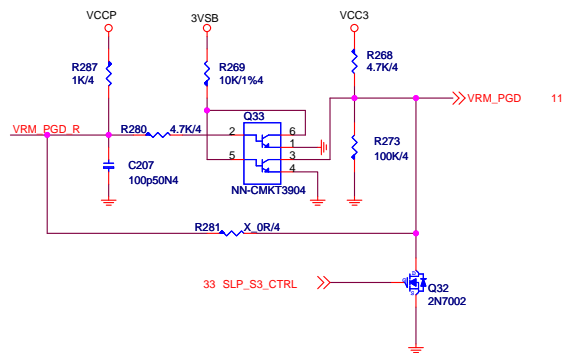


GPIO13 from PCH

TO ALL PCIE SLOT RESET#



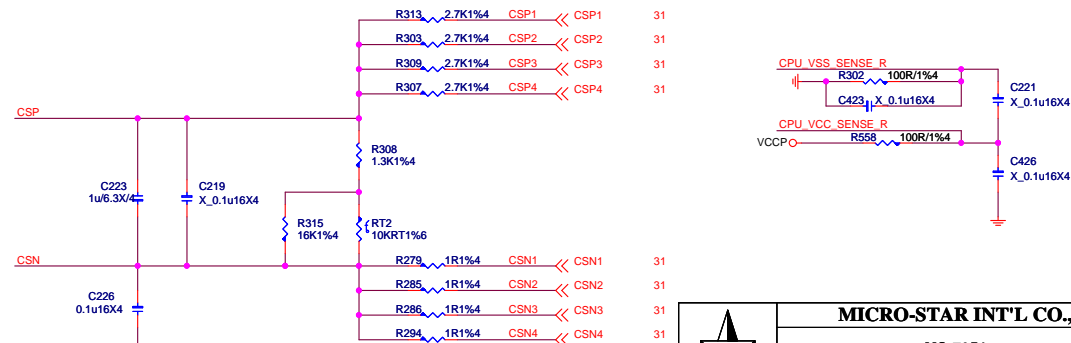
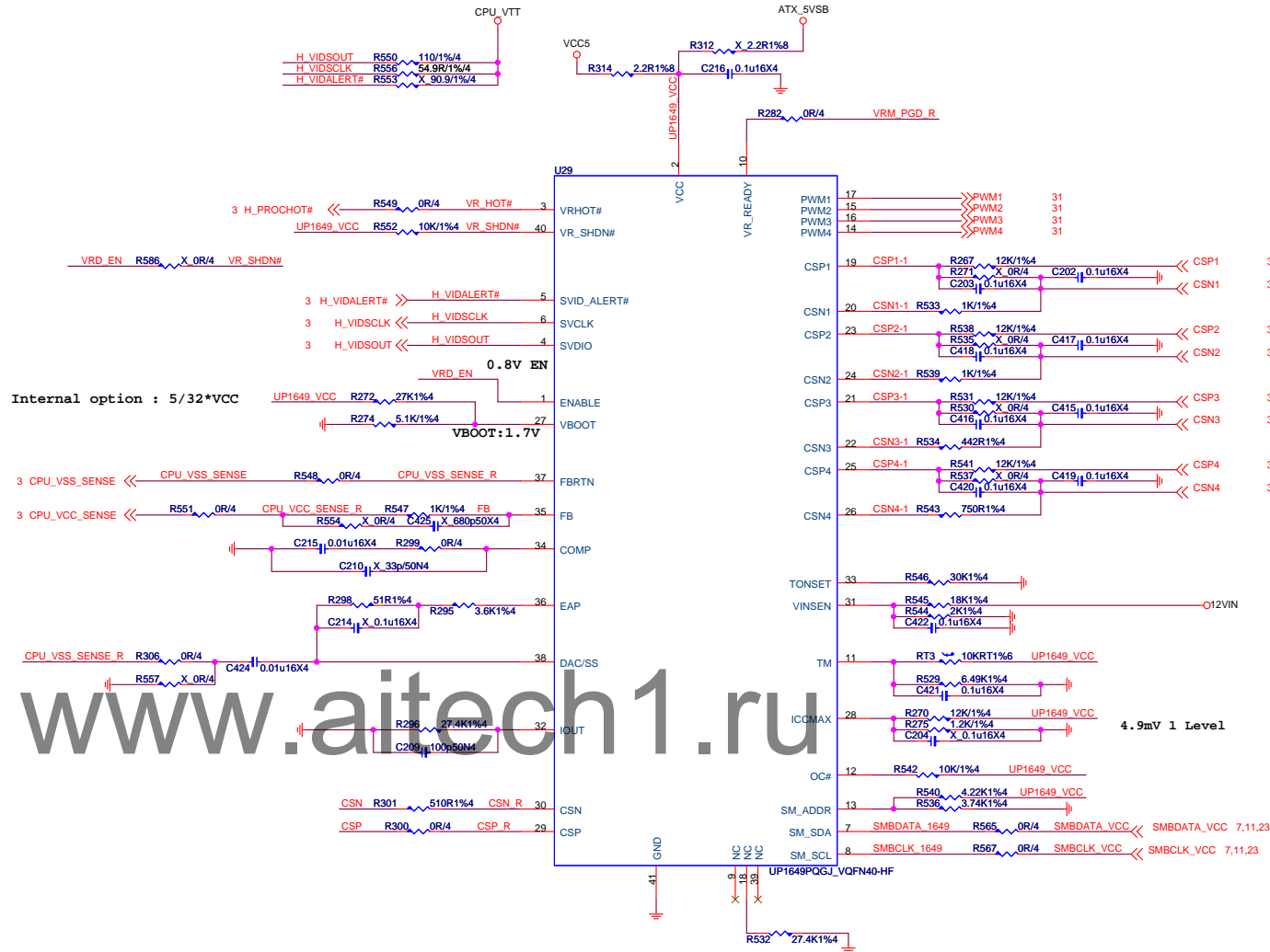
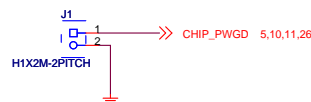
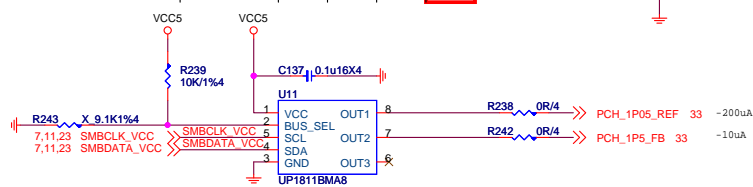
MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	ACPI controller UPI	10	
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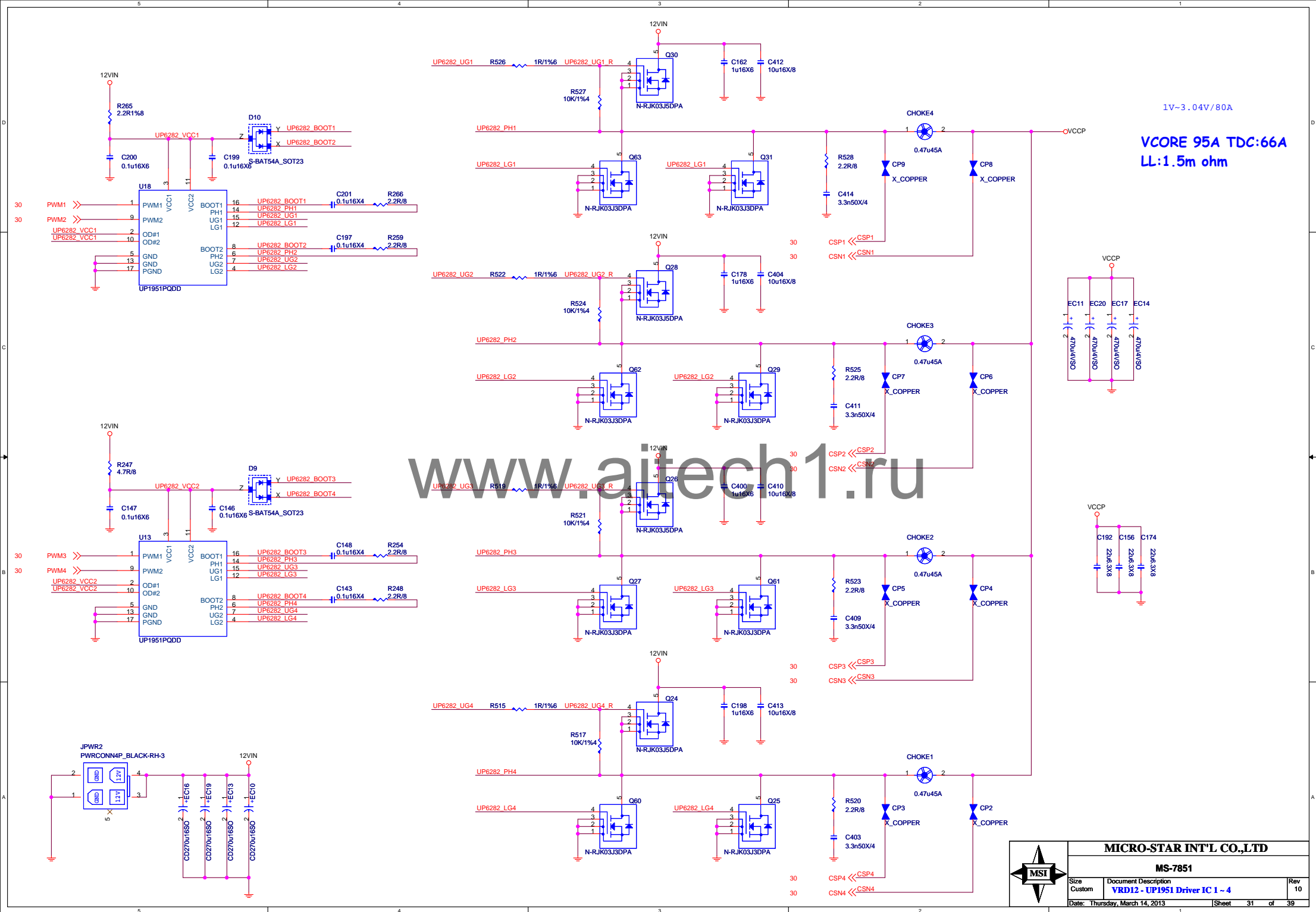


UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN


ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (Kohm)	OPEN	3.9	3	2.2	1.3	10
RL (Kohm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%





1V~3.04V/80A
VCORE 95A TDC:66A
LL:1.5m ohm

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Custom	VRD12 - UP1951 Driver IC 1 ~ 4	10
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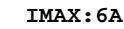
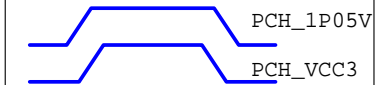
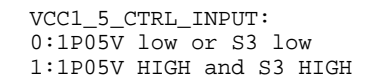
$R_{320}=14K\ ohm$

Size Custom	Document Description DDR POWER - UP1504S -2PHASE	Rev 10
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PCH Core 6A

$$I_{out \text{ ripple}} = 5A$$

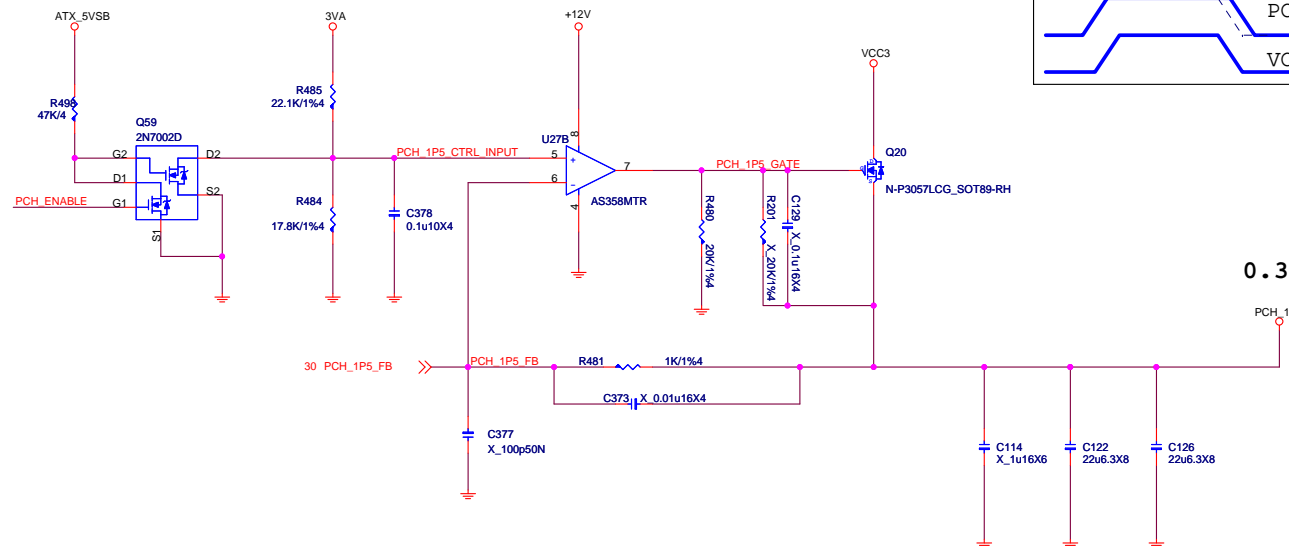
0.133A



PCH: 0.35A

$I_{max}: 0.35A$

0.35A

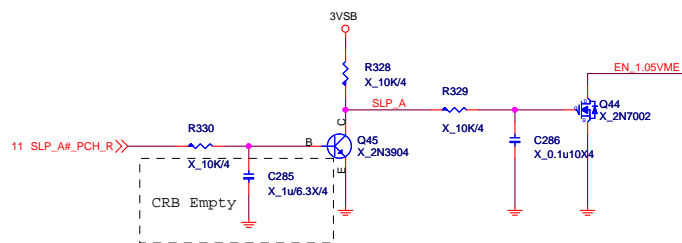


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Size Custom	Document Description PCH POWER - OP+MOS*2	Rev 10
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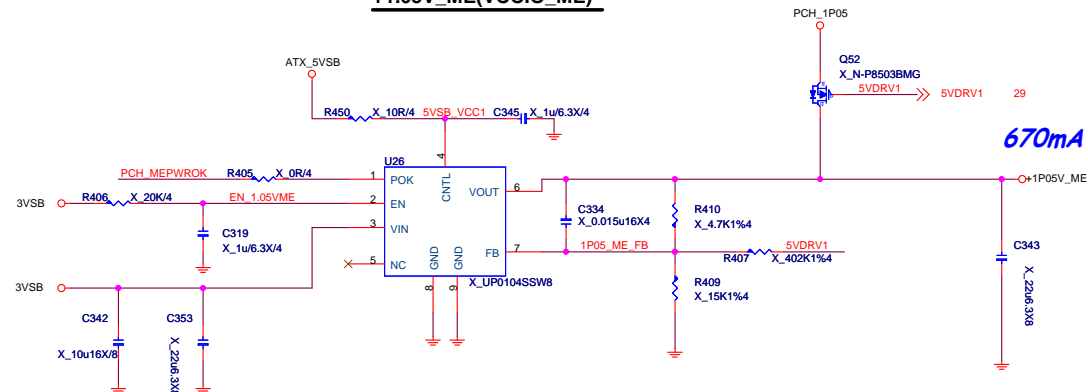
C318,C323,R378,C313,C314,C333,R366 for H87 un stuff
Z87 only stuff R354

SLP_A

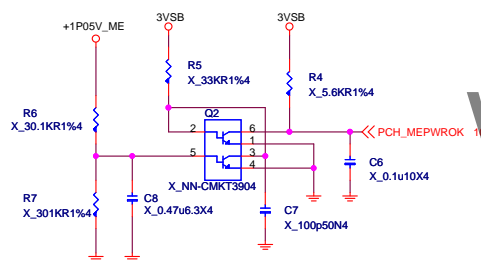


ME Power Control

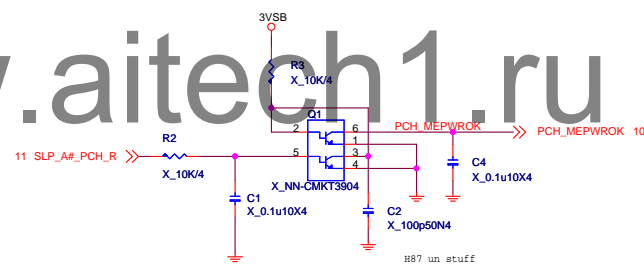
+1.05V_ME(VCCIO_ME)



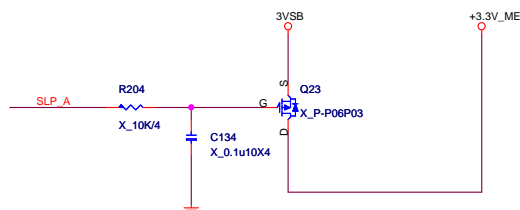
PCH_MEPWROK



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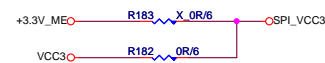


+3.3V_ME



For INTEL ME BUG

Z87->Stuff R654
H87 - B85->Stuff R653



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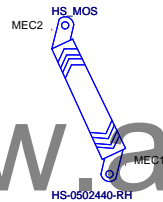
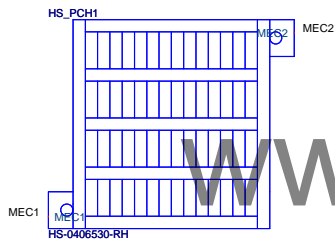
Size	Document Description	Rev
Custom	ME POWER	10
Date: Thursday, March 14, 2013	Sheet 34 of 39	



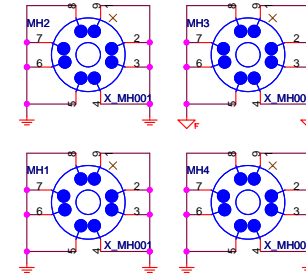
PD0-078510A-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)



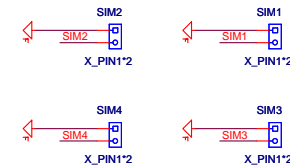
HEATSINK



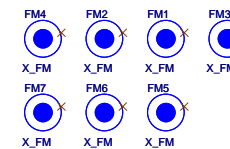
Mounting Holes



Simulation



Optical Fiducial Marks-120



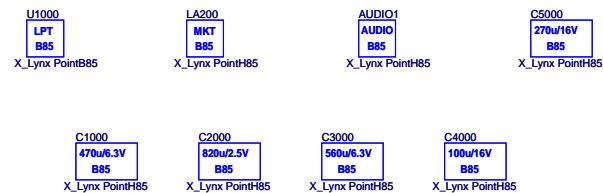
SPI OPT.



H87 OPT.

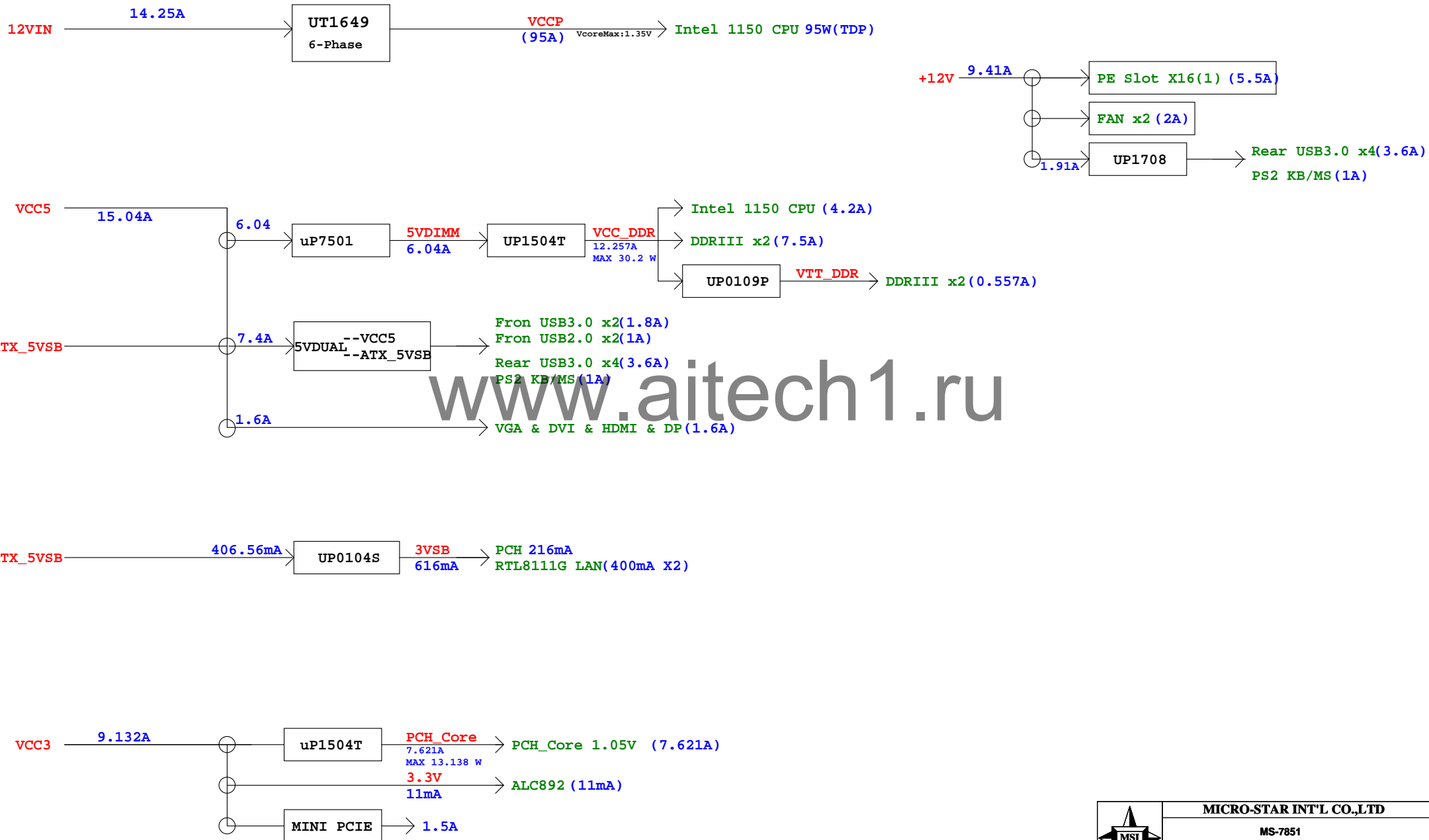


B85 OPT.



Power Delivery

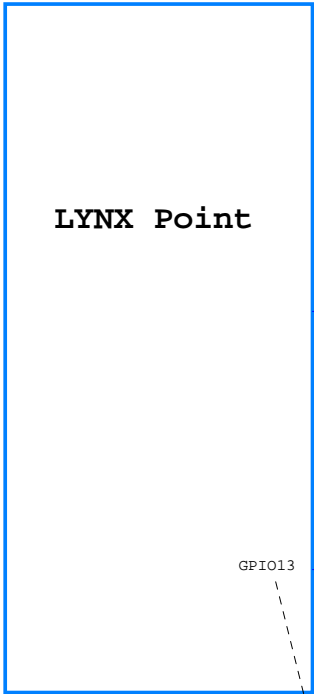
Slot



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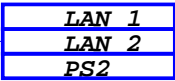
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LYNX Point

SB_WAKE#



LAN 1
LAN 2
PS2

EUP Disable
S4/S5 --> support PS2/PCIE Wake
S3 -->support PS2/USB/PCIE Wake

EUP Enable
S4/S5 -->not support any Wake
S3 -->support PS2/USB/PCIE Wake

GPIO13

SIO_PME#

PME#

SIO-NTC6779D

GP70 DSW_EN
GP71 ME_DIS#
GP72 USB_MODE
GP73 WDT#
GP25 AMDPWR_EN
GP36 mSATA_MINI_EN

For BIOS use

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(G3)DS5 ---> S0

VCCRSTC (MB-->PCH)

RTCRST# (MB-->PCH)

SYS3VSB_OFF (By SIO)

UP0104S 3VSB (By ATX_5VSB)

RSMRST# (By SIO to PCH) (SIO delay 200ms-300ms as VSB arrives at 3.033V)
up: 3.033V down:2.882V

PWRBTIN# (to SIO to PCH) (CP Internal 16ms debounce)

SLP_S5# (By PCH to ???)

SLP_S4# (By PCH to SIO)

SLP_S3# (By PCH to SIO)

PSON# (as S3) (By SIO to PS) (SIO delay 80ns By SLP_S3#)

12V/5V/3V (By PS to MB) (12/5V --->3V <=20ms)

uP7501 5VDRV1 (By S3 & S4 & 5V) (UP7501 delay 6ms-10ms)

uP7501 5VDIMM (By 5VDRV1)

uP1504 VCC_DDR (By 5VDIMM)

uP0109 VTT_DDR (By 5V & VCC_DDR to CPU)

OP+MOS*2 PCH_1P05 (by SLP_S3# & 12V & VCC_DDR)

UP7534 PCH_VCC3 (by SLP_S3# & PCH_1P05)

OP+MOS PCH_1P5 (by SLP_S3#)

VR_EN (By 12V & SLP_S3# & PCH_1P05)

VBOOT (1.7V) (By VR_EN<=5ms)

VRM_PGD (VR12.5 to PCH) (By VBOOT Ready <=100us)

ATX_PWR_OK (By PS to SIO 12V/5V/3V Delay 100ms-500ms)

CHIP_PGD(SIO_ATXOK)(SIO to PCH)(By ATX_PWR_OK & 3.3V<~2.83V) (delay 300~500ms)

MEM_PWRGD (By PCH to CPU) (as CHIP PGD & VR_READY) (CPU: 1ms min)

BCLK (as CHIP PGD)

CPUPWROK (PCH to CPU) (By BCLK) MIN 1ms MAX :100ms

VCCIO_OUT & VCOMP_OUT (By CPUPWROK)

SVID (VR12 to CPU) (By VR_EN Ready (>Vih)) (CPUPWROK之後delay500us output SVID)

UP1649 VCCP

VIDALERT# (By SVID Ready)

PLTRST# (PCH to CPU) (By PCH to CPU/SIO) (CPUPWROK to PLTRST 5ms max)

CPURST# (PCH to CPU) (By PLTRST#)

DMI#

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MS-7851-0A to 1.0 Modify history

- 1. Remove TPM connect .
- 2. Add COM port .
- 3. Remove C85,C88,R113,R133,R123,Q12,Q53 .
- 4. LANl_USB 3.0 TX0 TX1 change .
- 5. Change Q20 to "D03-3057L19-N03" for PCH power 1.5V .
- 6. Add R224 for PCH_PWRGD .
- 7. Q12 change to 2N7002 for CHIP_PWRGD .
- 8. Remove C171,168,165,177,181,184,188,EC8 for power solution .
- 9. Add R113,123 to DDR function.
- 10. Change D18 for SMBUS EMI solution .
- 11. Add R223 for GPIO37 .
- 12. HDMI levlshift change to NXP3360 .
- 13. Q53 change to 3904 .
- 14. Add OC#1 & OC#5 to from USB.
- 15. Remove +1P05_ME one 22u output cap .
- 16. Add 4.7u CL43~46 for surge improvement .

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Model	Sample BOM	chipset	Market Name
MS-7851 0A OPT:A	601-7851-A10	H87 chipset	H87-G51
MS-7851 0A OPT:B	601-7851-A20	Z87 chipset	Z87-G51